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DEVELOPMENT OF THE TEST UNIT FOR THE SATCOM SIGNAL ANALYZER

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The Satellite Communications Signal Analyzer (SSA) has been designed and constructed at the Naval Postgraduate School. Included in the SSA is a set of self-test and calibration subsystems, collectively known as the TEST UNIT. This report documents the design and construction of the TEST UNIT. It addresses design philosophy, technical design

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(20. ABSTRACT Continued)

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ABSTRACT

The Satellite Communications Signal Analyzer (SSA) has been designed and constructed at the Naval Postgraduate School. Included in the SSA is a set of self-test and calibration subsystems, collectively known as the TEST UNIT. This report documents the design and construction of the TEST UNIT. It addresses design philosophy, technical design aspects, test procedures and applications of the TEST UNIT in the SSA.

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I. INTRODUCTION

The Satcom Signal Analyzer (SSA) is a real-time signal processing system designed to monitor authorized users and to analyze RFI sources within Navy satellite communications systems. It provides multi-channel digital spectrum analysis with CRT graphics and hard copy output, AM, FM, PSK and FSK demodulation and recording, and phase-locked loop frequency measurement. It is controlled by a PDP-11/34 minicomputer. Reference 1 describes the digital control of the SSA. A simplified block diagram of the SSA is shown in Figure 1.1.

Signals received at the antennas are sent to the SSA RF Units for down-conversion and amplification. From there they go to the Signal Selection Unit which routes the signals to the various SSA receivers. The Frequency Receivers provide phase-locked loop carrier frequency measurement. The AN/WSC-3 provides demodulation of AM, FM, PSK and FSK signals, as well as transmit capabilities discussed in this report. The Spectrum Receivers provide signals to A/D converters for digital spectrum analysis. The Dual Graphics display, Hard Copy Unit, Analog Tape Recorder and X-Y Modulation display are the output devices used to monitor and analyze satellite communications signals [Reference 2].

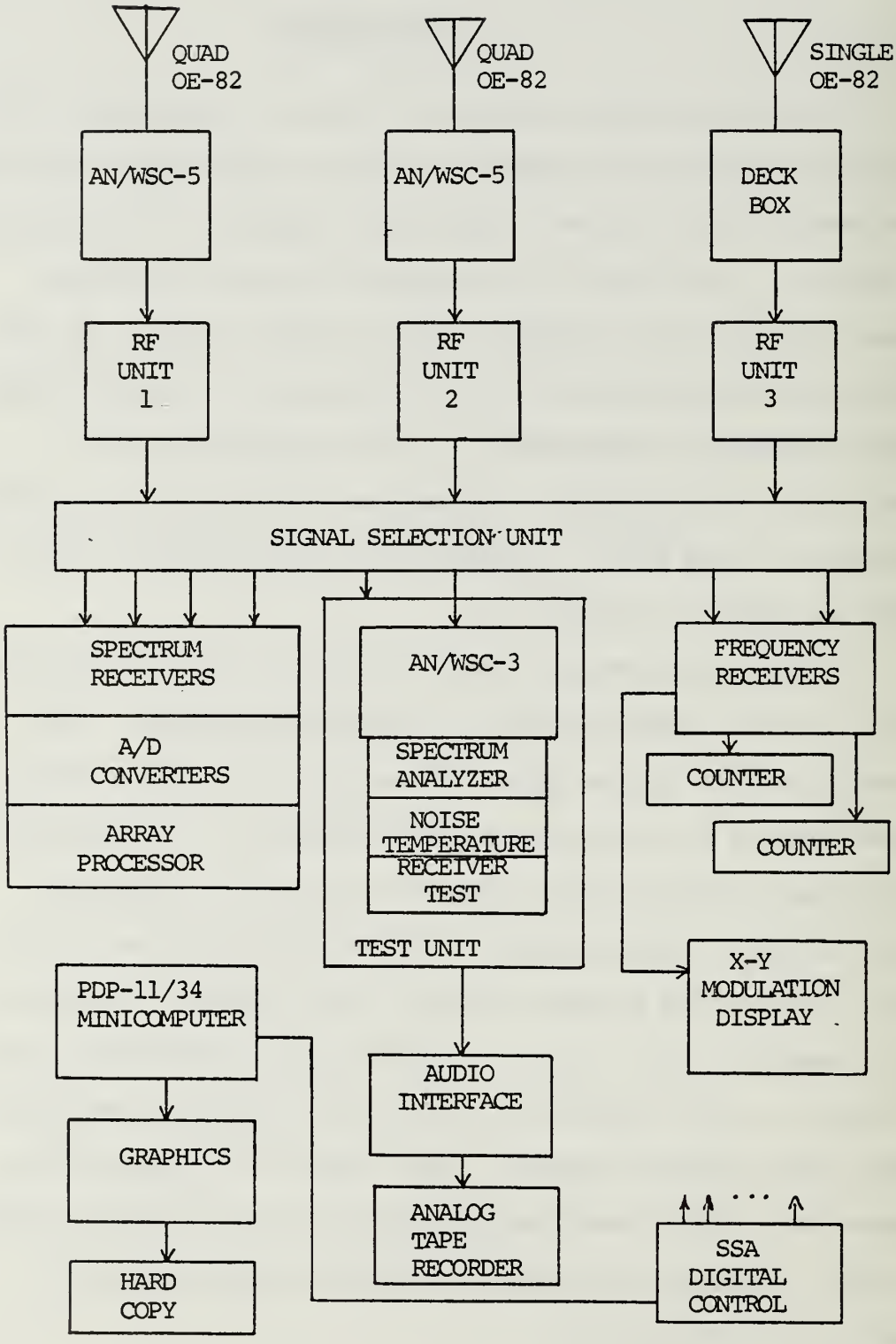


FIGURE 1.1. SSA BLOCK DIAGRAM.

The TEST UNIT is a collection of subsystems within the Satellite Communications Signal Analyzer (SSA hereafter), primarily devoted to self-test and calibration of the SSA. It provides the following capabilities and functions:

a) analog spectrum analysis of SSA signals

b) time domain (oscilloscope) display of SSA signals

c) operating noise temperature test

d) generation of test signals of precise amplitude, frequency and modulation format. These signals are injected into SSA receivers for testing and calibration.

e) power balancing, general up-conversion, and AM, FM, PSK and FSK signal reception using an AN/WSC-3 transceiver

f) bit error rate testing with a Hewlett-Packard HP1645A Data Error Analyzer.

The TEST UNIT is organized as follows: Spectrum Analyzer Section, Noise Temperature Section, Receiver Test Section, AN/WSC-3 Section and the Data Interface Section. Figure A.7, Appendix A, is a block diagram of the modules that make up the TEST UNIT and it shows the signals into and out of each module. The Spectrum Analyzer Section is located on modules TU and TR. Also contained on TR is the Receiver Test Section. The Noise Temperature Section is located on TUI and WP. The AN/WSC-3 Section consists of WP, RT and RS. The Data Interface Section consists of DI, BE and WP.

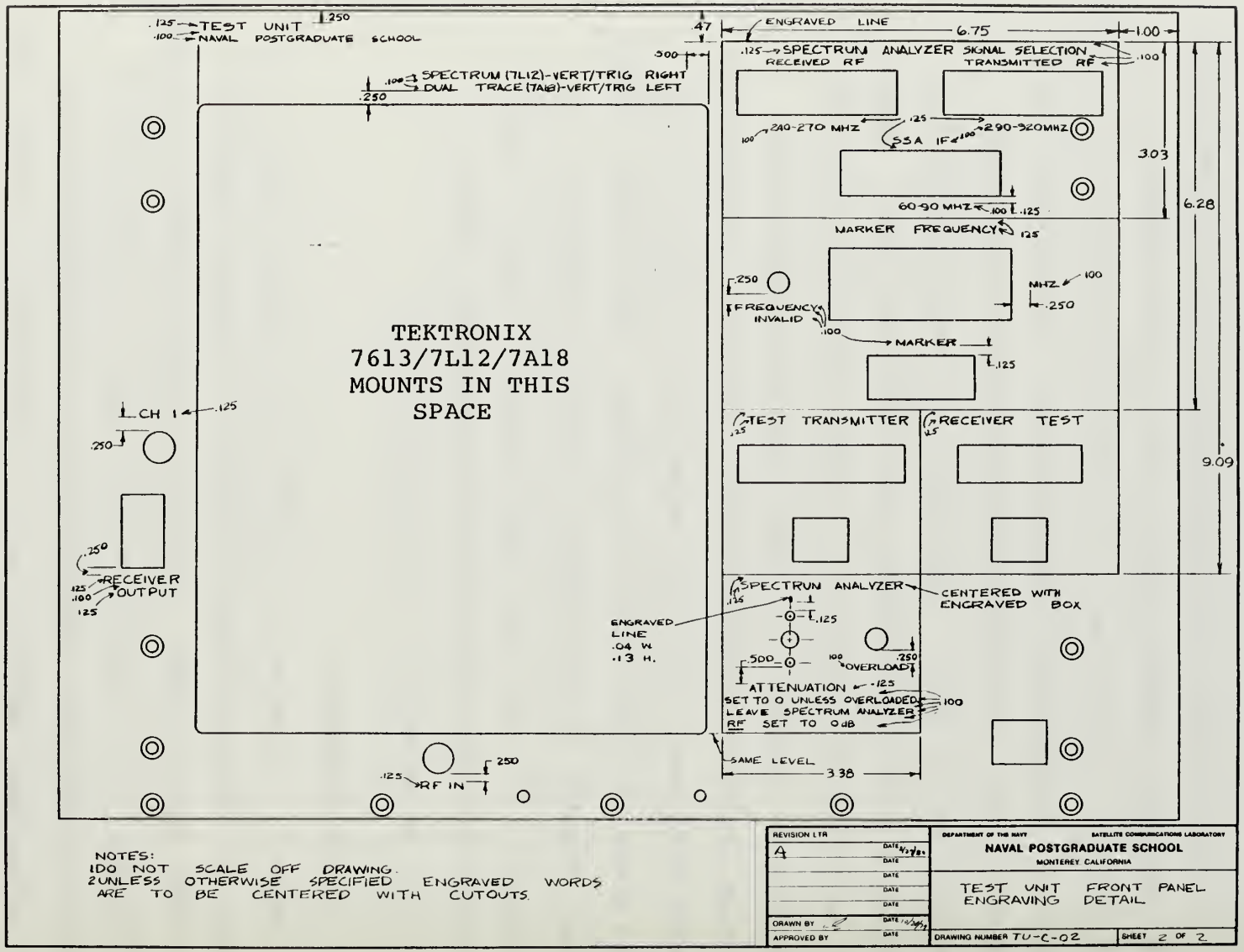
The design, construction and application of each of the TEST UNIT sections and their interaction within the TEST UNIT and the SSA are described in this report.

II. SPECTRUM ANALYZER SECTION

The SSA provides real time spectrum analysis using digital techniques implementing the Fast Fourier Transform; two CRT graphics displays and a hard-copy unit display the resulting spectra. The TEST UNIT supplements this SSA feature with a Tektronix 7613 mainframe oscilloscope and 7L12 spectrum analyzer plug-in unit. SSA signals are automatically displayed on the 7613 selected on the TEST UNIT panel. Figure 2.1 describes the layout of the TEST UNIT panel which houses the spectrum analyzer and signal selection pushbuttons. Precise frequency comparison may be made with an adjustable Marker Frequency which, when selected, is coupled into the 7613 along with the signal of interest. Additionally, time-domain display of SSA signals is possible through use of a Tektronix 7A18 dual-trace amplifier plug-in unit. Signals from the five SSA receivers are automatically routed to the 7A18 as selected on the TEST UNIT panel.

A. SIGNAL SELECTION

Signals are routed to the 7613 for spectrum analysis via a pair of LORCH electronic switches, S3 and S4, mounted on the TEST UNIT RF panel. Control of these switches is provided by digital logic circuits on Test Board II, located behind the TEST UNIT panel; manual selection of a specific signal is accomplished through a set of pushbuttons on the TEST UNIT panel. The nine pushbuttons are labeled as follows:



NOTES:
1. DO NOT SCALE OFF DRAWING.
2. UNLESS OTHERWISE SPECIFIED ENGRAVED WORDS ARE TO BE CENTERED WITH CUTOUTS.

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TEST UNIT FRONT PANEL ENGRAVING DETAIL

DRAWING NUMBER TU-C-02 — SHEET 2 OF 2

FIGURE 2.1

1. Received RF
    a. Antenna 1 (AN/WSC-5)
    b. Antenna 2 (AN/WSC-5)
    c. Antenna 3 (SSA)
2. Transmitted RF
    a. Antenna 1 (AN/WSC-5)
    b. Antenna 2 (AN/WSC-5)
    c. Antenna 3 (SSA)
3. SSA IF
    a. Antenna 1
    b. Antenna 2
    c. Antenna 3

The selection of one of these nine momentary switches on the TEST UNIT panel is detected by a priority encoder. See Figure A.2, Appendix A. The resulting BCD code is latched, then decoded. The nine output lines of the BCD decoder are used to control the LORCH switches and to light a lamp beneath the selected pushbutton. This arrangement allows the selection of a different signal through a single pushbutton selection.

The logic circuits required for signal selection are located on Test Board II. See Figure A.2, Sheet 3, Appendix A. U4 provides pull-up resistors for the switches on the TEST UNIT panel. U1, 74148, encodes eight of the nine switches into a three-bit BCD code, which is latched by U3, 74175. The ninth switch is connected directly to the most significant bit of the latch. Thus, the closing of one of the

nine momentary switches results in a unique four-bit code being latched in U3 until another switch is depressed. This four-bit code is then decoded into one of nine control lines by U6, 7442. The control line associated with each switch activates the respective indicator lamp on the TEST UNIT panel as well as the corresponding switch. Table 2.1 lists a truth table for this logic. Lamp control is discussed in Chapter VIII.

Signals for the Spectrum Analyzer Section enter the TEST UNIT at the TEST UNIT RF panel (TR), from the SSA RF Units and Signal Selection Unit. These nine signals are applied to a pair of LORCH electronic switches whose control comes from U6 on Test Board II as explained previously. The variable attenuators are explained in Section II.D. The selected signal is amplified, a sample is coupled off for overload detection, then the signal is coupled into the Tektronix spectrum analyzer. At this point, the frequency marker is added, if selected. See Figure 2.2 for a block diagram of this section.

Any very strong signal entering the Spectrum Analyzer section could saturate the Tektronix 7L12. Such an overload condition is detected by coupling off a sample of the input signal at CP 3, converting the RF power to a DC voltage with a Schottky-diode detector (DET 2) and comparing this voltage with some nominal reference voltage in the OVERLOAD DETECTOR (A1). If this DC voltage (and hence, the RF power) exceeds the nominal value, an indicator is lighted on the TEST UNIT

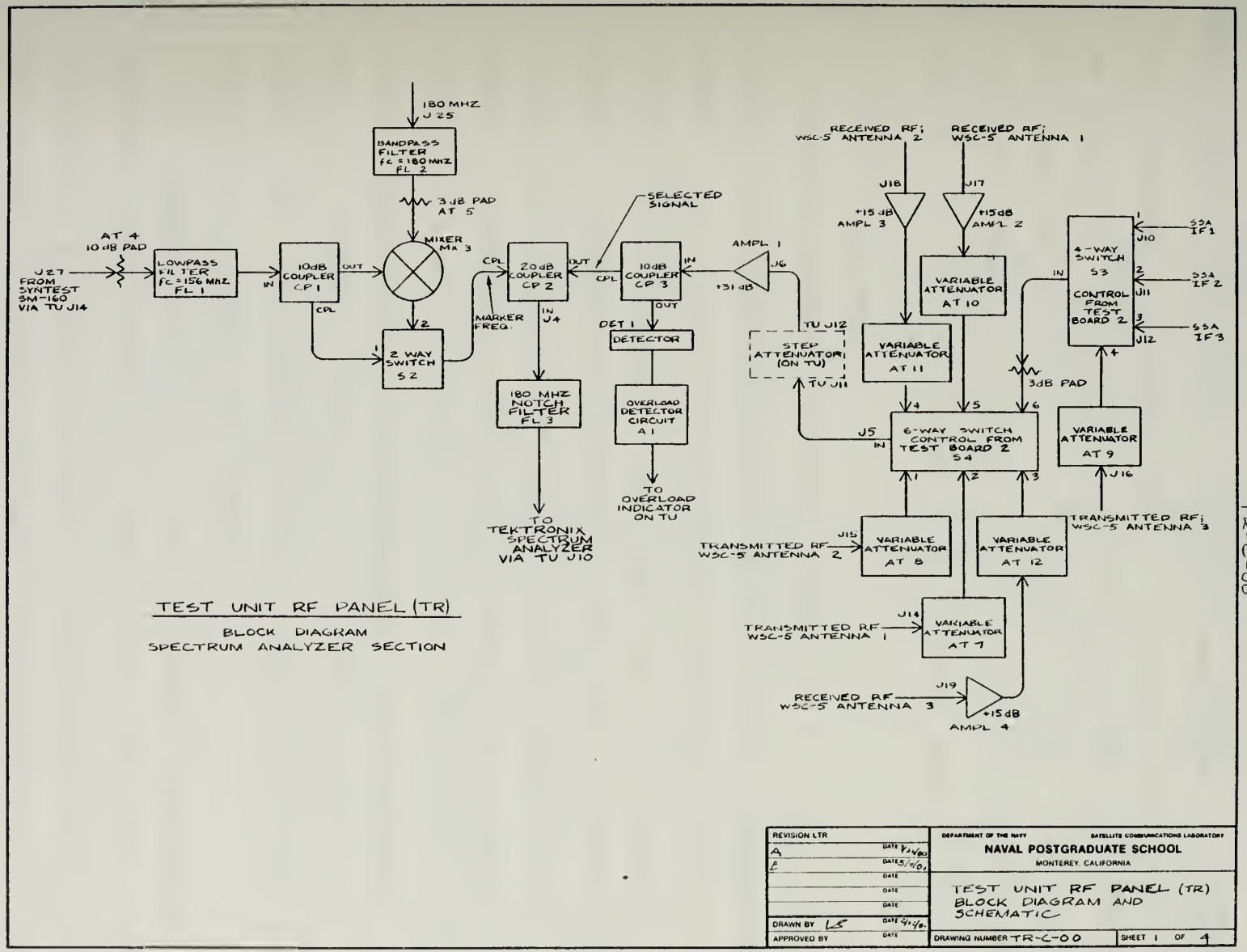

180 MHZ
J 25
BANDPASS FILTER fc = 180 MHZ FL 2
3 dB PAD AT 5
SELECTED SIGNAL
AT 4 10 dB PAD
J27 FROM SYNTEST SM-160 VIA TU J14
LOWPASS FILTER fc = 156 MHZ FL 1
10dB COUPLER CP 1
MIXER Mx 3
2 WAY SWITCH S2
MARKER FREQ.
20 dB COUPLER CP 2
10dB COUPLER CP 3
DET 1
DETECTOR
180 MHZ NOTCH FILTER FL 3
OVERLOAD DETECTOR CIRCUIT A1
TO TEKTRONIX SPECTRUM ANALYZER VIA TU J10
TO OVERLOAD INDICATOR ON TU
AMPL 1 J6 +31 dB
STEP ATTENUATOR (ON TU)
TU J12
TU J11
RECEIVED RF; WSC-5 ANTENNA 2
RECEIVED RF; WSC-5 ANTENNA 1
J18
J17
+15 dB AMPL 3
+15dB AMPL 2
VARIABLE ATTENUATOR AT 10
VARIABLE ATTENUATOR AT 11
4-WAY SWITCH S3 CONTROL FROM TEST BOARD 2
J10
J11
J12
S3A IF 1
S3A IF 2
S3A IF 3
3dB PAD
J5
6-WAY SWITCH CONTROL FROM TEST BOARD 2 S4
VARIABLE ATTENUATOR AT 9
J16
TRANSMITTED RF; WSC-5 ANTENNA 3
TRANSMITTED RF WSC-5 ANTENNA 2
J15
VARIABLE ATTENUATOR AT 8
VARIABLE ATTENUATOR AT 12
TRANSMITTED RF WSC-5 ANTENNA 1
J14
VARIABLE ATTENUATOR AT 7
RECEIVED RF WSC-5 ANTENNA 3
J19
+15dB AMPL 4
TEST UNIT RF PANEL (TR)
BLOCK DIAGRAM
SPECTRUM ANALYZER SECTION
REVISION LTR
A DATE 9/14/80
B DATE 5/11/81
DRAWN BY LS DATE 4/14/80
APPROVED BY
DEPARTMENT OF THE NAVY SATELLITE COMMUNICATIONS LABORATORY
NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA
TEST UNIT RF PANEL (TR) BLOCK DIAGRAM AND SCHEMATIC
DRAWING NUMBER TR-C-00
SHEET 1 OF 4

FIGURE 2.2

TABLE 2.1

BUTTON	74148 PIRORITY ENCODER INPUT	A2	A1	A0	74175 LATCH Q4	Q3	Q2	Q1	7442 SELECTED LINE
RCV ANT 1	10	H	H	H	L	L	L	L	0
RCV ANT 2	11	H	H	L	L	L	L	H	1
RCV ANT 3	12	H	L	H	L	L	H	L	2
XMIT ANT 1	13	H	L	L	L	L	H	H	3
AMIT ANT 2	1	L	H	H	L	H	L	L	4
IF 1	2	L	H	L	L	H	L	H	5
IF 2	3	L	L	H	L	H	H	L	6
IF 3	4	L	L	L	L	H	H	H	7
XMIT ANT 3	X	H	H	H	H	L	L	L	8

panel. The OVERLOAD DETECTOR is adjusted so that a signal of -20 dbm or more into the spectrum analyzer will light the indicator. A step attenuator is mounted on the panel and electrically precedes AMPL 1. If an overlaod condition is indicated, the operator should increase attentuation until the indicator turns off. See Figures A.6 and A.9 in Appendix A for schematic diagrams of the overload detector and the spectrum analyzer selection of the TEST UNIT RF panel.

B. MARKER FREQUENCY

A Syntest SM-160 frequency synthesizer is located behind the TEST UNIT panel for generation of a precise marker frequency. This marker is selected via the Marker ON-OFF switch on the TEST UNIT panel. (See Figure 2.1.) BCD frequency control is provided to the SM-160 via a set of thumbwheels on the TEST UNIT panel and digital logic circuits on Test Board I. Selection of an invalid frequency is detected on Test Board I and signaled by a flashing LED located adjacent to the thumbwheels. (Valid frequencies are those only in the ranges of 60 - 99.999 MHz, 240 - 279.999 MHz, and 290 - 329.999 MHz.) A schematic diagram of Test Board 1 is shown in Figure A.1, Sheet 1-3, Appendix A.

The Syntest SM-160 is a 5 digit frequency synthesizer providing ECL signals in the range of 20 to 160 MHz at +2dbm. Selection of a frequency between 60 and 90 MHz results in control bits for these frequencies to be present at the input to the SM-160. All other valid marker frequencies fall

outside the range of this device. In this case, valid thumbwheel selection results in a frequency out of the SM-160 that, when mixed with 180 MHz, provides a signal at the selected frequency. A read-only memory (U22, 74186) on Test Board I senses the thumbwheel setting and provides BCD control resulting in the correct SM-160 frequency. (Table 2.2 lists thumbwheel settings and corresponding SM-160 output. Table 2.3 lists PROM programming to achieve the desired frequency.) The resulting output is lowpass filtered, FL1, Figure 2.2, to remove the ECL harmonics, and the output is split by CP1. The coupled portion goes directly to a LORCH electronic switch (S2) and the output portion is mixed with a 180 MHz signal in MX3 and then is applied to the same switch. When the marker is selected, the logic on Test Board I determines which input to the LORCH switch is coupled into the spectrum analyzer. See Figure 2.2. Coupler CP2 combines the selected signal and marker for input to the 7L12. Filter FL3 removes the robust 180 MHz signal component.

C. TIME DOMAIN SIGNAL DISPLAY

Signals from the four SSA Spectrum Receivers and from the AN/WSC-3 are routed to the 7613 oscilloscope via the Audio Selector. A single thumbwheel is located on the TEST UNIT panel to the left of the 7613 and provides three control lines to the Audio Selector. See Figure 2.1. Table 2.4 lists thumbwheel settings, resulting BCD codes and the corresponding receiver outputs. The selected signal is routed

TABLE 2.2

Thumbwheel Selection and SM-160 Output

HUNDREDS MHz THUMBWHEEL POSITION	$\overline{8}\overline{4}\overline{2}\overline{1}$	TENS MHz THUMBWHEEL POSITION	$\overline{8}\overline{4}\overline{2}\overline{1}$	SM-160 OUTPUT
0	LLLL	6	LHHL	60 - 69.999 MHz
0	LLLL	7	LHHH	70 - 79.999 MHz
0	LLLL	8	HLLL	80 - 89.999 MHz
0	LLLL	9	HLLH	90 - 99.999 MHz
2	LLHL	4	LHLL	*60 - 69.999 MHz
2	LLHL	5	LHLH	*70 - 79.999 MHz
2	LLHL	6	LHHL	*80 - 89.999 MHz
2	LLHL	7	LHHL	*90 - 99.999 MHz
2	LLHL	9	HLLH	*110 - 119.999 MHz
3	LLHH	0	LLLL	*120 - 129.999 MHz
3	LLHH	1	LLLH	*130 - 139.999 MHz
3	LLHH	2	LLHL	*140 - 149.999 MHz

* These are mixed (up converted) with 180 MHz to produce 240 - 270 or 290- 320 MHz

TABLE 2.3 (From Ref. 1)

PROM PROGRAMMING

74186 FUZEABLE LINK PROM
64 WORDS x 8 BITS

PROM ADDRESS (HEX)	PROM OUTPUT (HEX)
06	31
07	39
08	41
09	49
24	31
25	39
26	41
27	49
29	89
30	91
31	99
32	A1

ALL OTHER ADDRESSES HAVE OUTPUT = 00 (HEX)

PROGRAMMING IS ACCOMPLISHED WITH A PRO-LOG PM-9055

TABLE 2.4

Receiver Output Selection

THUMBWHEEL POSITION	THUMBWHEEL OUTPUT	SELECTED RECEIVER
	8421	
1	HHHL	Spectrum Receiver 1 IF
2	HHLH	Spectrum Receiver 2 IF
3	HHLL	Spectrum Receiver 3 IF
4	HLHH	Spectrum Receiver 4 IF
5	HLHL	AN/WSC-3 Audio

to the 7A18 Dual-trace amplifier from AS J7 and is displayed on the 7613 scope. The operator must choose which plug-in module controls the 7613 mainframe; either the 7A18 Dual-trace amplifier or the 7L12 spectrum analyzer. Selection is made by the Vertical Mode and Trigger Source buttons on the 7613 mainframe. Choosing LEFT on both of these buttons selects the dual-trace amplifier; choosing RIGHT selects the spectrum analyzer.

D. ADJUSTMENTS

There are two types of adjustments that are required in The Spectrum Analyzer Section. These are the reference for the overload detector, and the gain of the input signals.

1. Overload Detector

See Figure A.6 in Appendix A for a schematic of the overload detector. A potentiometer (R4) provides the reference voltage at the input to the comparator (U1, NE 527) shown in the circuit. To adjust, apply a -10 dbm signal to the input of the HP33330B detector. Adjust the potentiometer until the overload indicator (LED) on the TEST UNIT panel begins to flicker on and off.

2. Signal Gain

The transmitted RF and received RF signal samples are each routed through slightly different paths; hence, two signals that appear at the same level on the spectrum analyzer may indeed be of different power. It is desirable to be able to observe a signal on the spectrum analyzer and add a single

correction factor to determine that signals' power at the antenna. Further it is desirable that this correction factor (in dB) be the same for all signal paths and that it be some integer multiple of 10 dB. For this reason a variable attenuator is provided on each of the RF signal inputs to the Spectrum Analyzer Section. To adjust, set the attenuator on the TEST UNIT panel to zero then proceed as follows:

a. Received RF

Tune the spectrum analyzer to 260 MHz. Apply a 260 MHz, -95 dBm signal to the input of the RF preamplifier in the deck box for Antenna 1. Generation of test signals is discussed in Chapter IV. Select the Received RF, ANT 1 push-button on the TEST UNIT panel. Adjust the variable attenuator associated with Antenna 1, AT10 (see Figure 2.2) until the 260 MHz signal is 25 dB down from the reference level on the spectrum analyzer display. Repeat this procedure for Antennas 2 and 3, using variable attenuators AT11 (ANT 2) and AT12 (ANT 3). Thereafter, signal power at the antenna preamp can be found by subtracting 40 dB from the level observed on the spectrum analyzer.

b. Transmitted RF

Tune the SSA's AN/WSC-3 transceiver to a legitimate transmit frequency that is not used by any local communications network. Transmit a 10 dbW, CW signal through Antenna 1. Instructions for the use of the AN/WSC-3 are discussed in Chapter V and Appendix G. Tune the 7L12 spectrum analyzer

to the same transmit frequency and select the TRANSMITTED RF, ANT 1 pushbutton on the TEST UNIT panel. Adjust variable attenuator AT7 (see Figure 2.2) until the signal observed on the spectrum analyzer is 10 dB down from the reference line on the display. Repeat for Antennas 2 and 3 using AT8 (ANT 2) and AT9 (ANT 3). Thereafter, the reference line on the spectrum analyzer corresponds to a 20 dbW actual transmit power (not EIRP).

III. NOISE TEMPERATURE SECTION

A. DESIGN ASPECTS

The purpose of the Noise Temperature Section is to provide a means for the operator to measure system operating temperature down through receiver RF or through receiver IF. Such a measurement requires an accurate noise generator and an indicator or sensor. Direct-reading noise figure instrumentation is commercially available. However, by employing the Y-factor technique of operating temperature measurement, use can be made of the SSA's intrinsic spectrum analysis capability.

In the Y-factor technique, a noise generator is connected to the input of the system and the resulting change in output noise power is observed. This change in output noise power is called the Y-factor. The relationship between operating temperature and the Y-factor may be derived as follows.

k = Boltzman's constant

P_1 = output noise power, with noise generator OFF

P_2 = output noise power, with noise generator ON

T_{op} = operating temperature

T_E = excess temperature of the noise generator, referenced to the preamplifier

Y = Y-factor due to the noise generator

B = bandwidth

G = gain

$$P_1 = kT_{op}BG \tag{3.1}$$

$$P_2 = k(T_{op} + T_E)BG \tag{3.2}$$

$$Y = \frac{P_2}{P_1} = \frac{T_{op} + T_E}{T_{op}} \tag{3.3}$$

$$T_{op} = \frac{T_E}{Y-1} \tag{3.4}$$

Thus, knowing T_E and having observed Y, the operator (or CPU) can calculate the system operating temperature.

The block diagram for the Noise Temperature Section is shown in Fig. 3.1. The equipment shown is duplicated for each of three antennas. The noise generator is energized by applying 28 VDC to its input terminals. This power is applied via a relay controlled by a bit from Control Bus Latch Board 12 (CBL12). When the noise temperature test for a specific antenna is selected, the corresponding control bit goes low, pulling in the relay contacts. Twenty eight VDC is routed through the relay to the noise generator. The resulting noise power is coupled with the antenna ouput, into the RF preamplifier and on to the SSA RF units. It is important that the conduct of the noise temperature test does not interfere with normal reception of satellite communications signals in the communication station. For this reason, the noise power is bandlimited to a frequency range within the RF passband that is not utilized by Navy Satellite

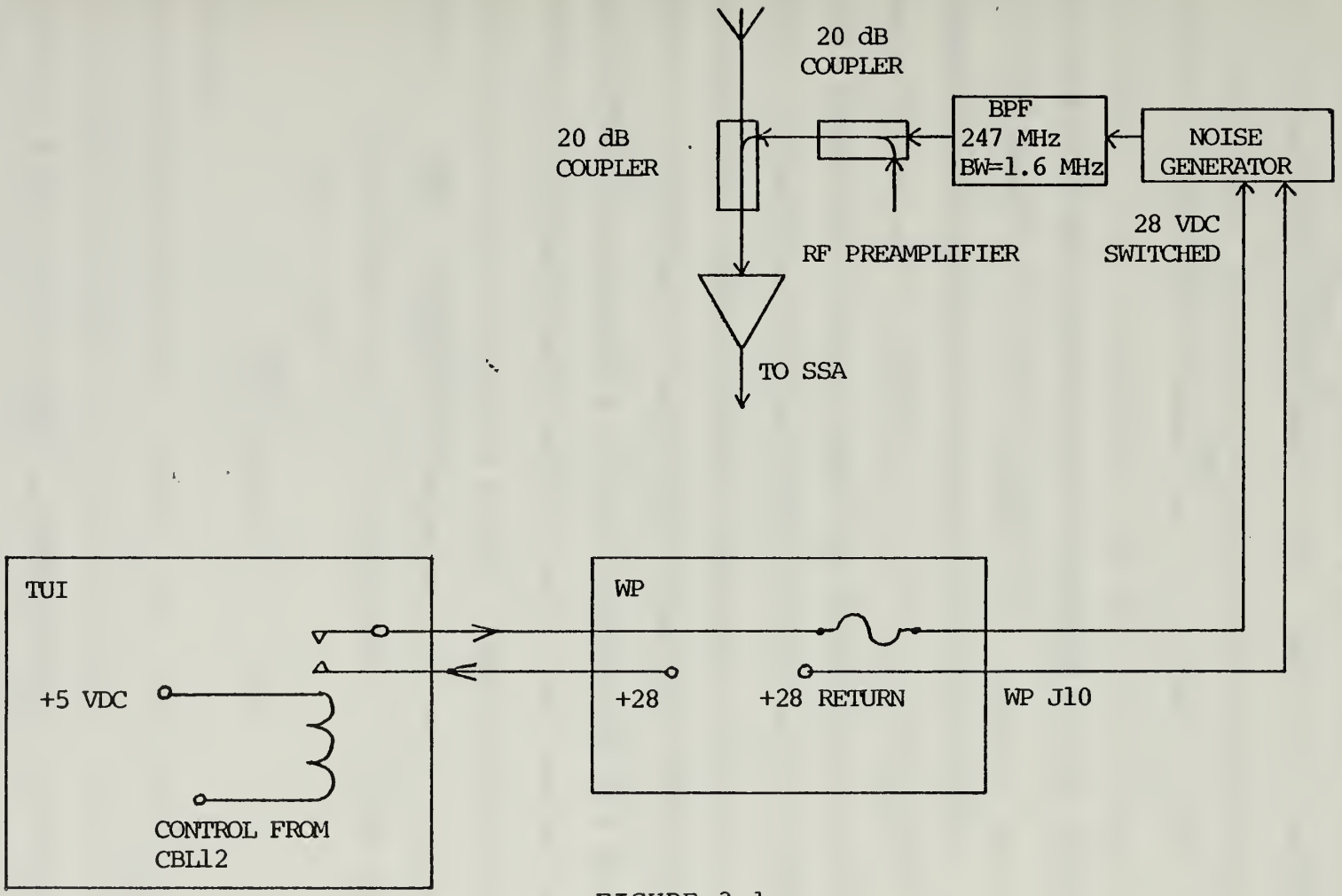

20 dB
COUPLER
20 dB
COUPLER
BPF
247 MHz
BW=1.6 MHz
NOISE
GENERATOR
28 VDC
SWITCHED
RF PREAMPLIFIER
TO SSA
TUI
+5 VDC
CONTROL FROM
CBL12
WP
+28
+28 RETURN
WP J10

FIGURE 3.1

Communications. This is accomplished by filtering the noise generator output with a bandpass filter of bandwidth 1.6 MHz, centered at 247 MHz. This added noise power results in a Y-factor seen at the input and output of the RF units of the SSA. This Y-factor is then sensed by the array processor and passed to the CPU for calculation, or it is observed manually by the operator utilizing the TEST UNIT Spectrum Analyzer Section. The operator enters his observation as the input to the CPU which then calculates operating temperature.

As seen by Equ. 3.4, calculation of operating temperature requires knowledge of the temperature of the noise generator as seen at the input to the preamplifier shown in Figure 3.1. This factor is determined once and entered into the noise temperature calculation algorithm at the time of initial set-up and calibration. T_E is a function of the coupling loss between the output of the noise generator and the input to the preamplifier, and of a specification of the noise generator known as the Excess Noise Ratio (ENR). Excess Noise Ratio is specified in dB and is defined as:

$$ENR = 10 \log_{10}\left(\frac{T_{ON}}{T_0} - 1\right) \tag{3.5}$$

Thus,

$$10^{(0.1)ENR} = \frac{T_{ON}}{290} - 1 \tag{3.6}$$

$$T_{ON} = 290(10^{(0.1)ENR} + 1) \tag{3.7}$$

Finally,

$$T_E = \frac{T_{ON} - T_O}{C} \tag{3.8}$$

$$T_E = \frac{T_O}{C} 10^{(0.1)ENR} \tag{3.9}$$

where C is the coupling loss from the output of the noise generator to the input of the preamplifier.

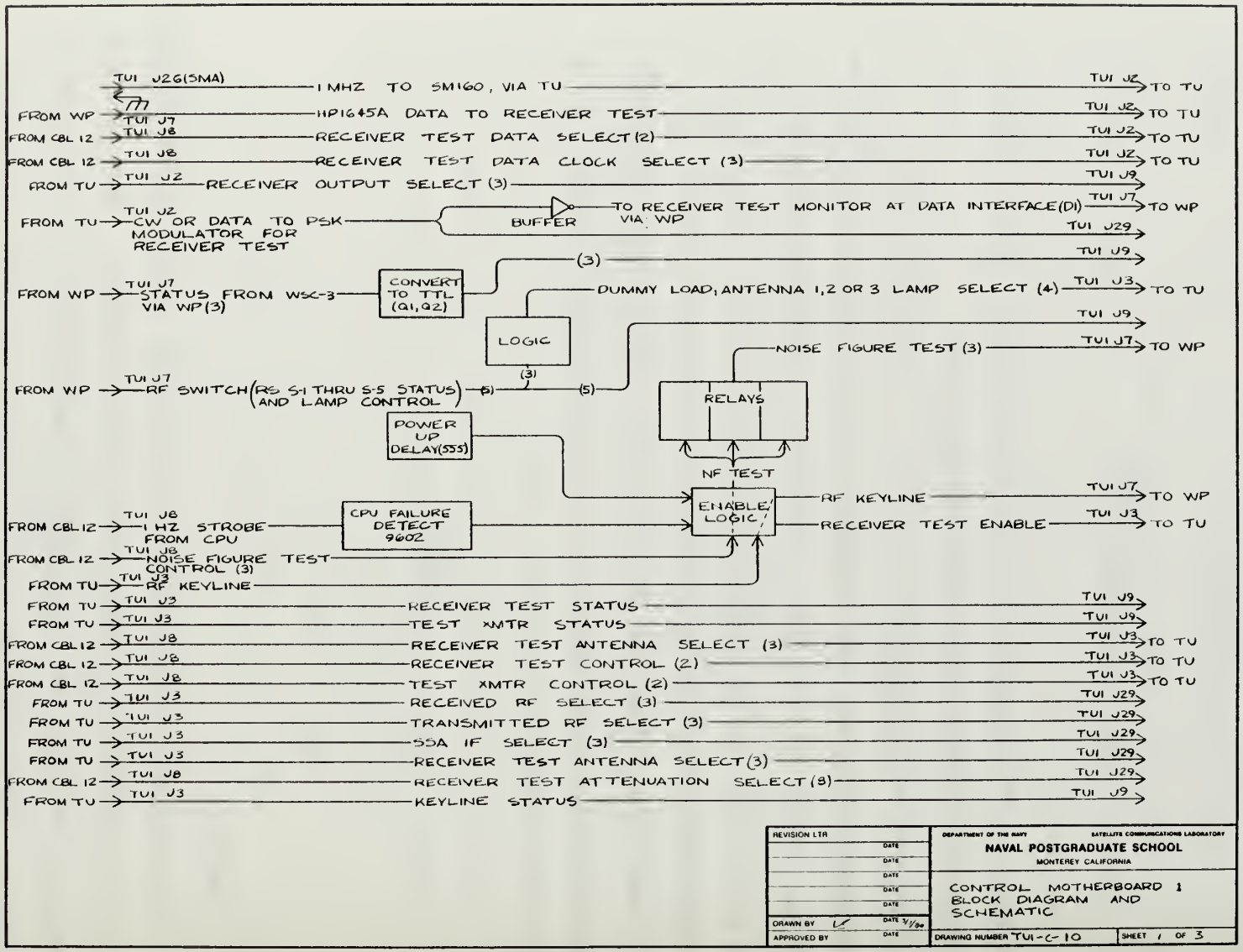
The operating temperature test is clarified by the following example. For Antenna 3 at the Naval Postgraduate School, the coupling loss, C, has been measured as 26.5 dB. The ENR of the noise generator associated with that antenna is specified as 35.4 dB. From Equ. 3.9, T_E = 2251.1 °K. Utilizing the Tektronix 7L12 spectrum analyzer in the TEST UNIT and energizing the noise generator, the Y-factor is observed as 6.5 dB. From Equ. 3.4,

$$T_{op} = \frac{2251.1}{10^{0.65} - 1}$$

$$T_{op} = 649.3 \text{ °K}$$

B. CONTROL

As previously mentioned, the DC power to the noise generator is provided by a relay controlled by CBL12. The circuits that provide this control are located on Control Motherboard I (CMB-I). Figure 3.2 is a block diagram of CMB-I; a schematic


TUI J26(SMA)
1 MHZ TO SM160, VIA TU
TUI J2
TO TU
FROM WP
TUI J7
HP1645A DATA TO RECEIVER TEST
FROM CBL 12
TUI J8
RECEIVER TEST DATA SELECT (2)
RECEIVER TEST DATA CLOCK SELECT (3)
FROM TU
TUI J2
RECEIVER OUTPUT SELECT (3)
TUI J9
CW OR DATA TO PSK MODULATOR FOR RECEIVER TEST
BUFFER
TO RECEIVER TEST MONITOR AT DATA INTERFACE (DI)
VIA WP
TUI J7
TO WP
TUI J29
(3)
CONVERT TO TTL (Q1, Q2)
STATUS FROM WSC-3 VIA WP (3)
DUMMY LOAD; ANTENNA 1,2 OR 3 LAMP SELECT (4)
TUI J3
LOGIC
NOISE FIGURE TEST (3)
RF SWITCH (RS S-1 THRU S-5 STATUS AND LAMP CONTROL)
(5)
RELAYS
POWER UP DELAY (555)
NF TEST
ENABLE LOGIC
RF KEYLINE
RECEIVER TEST ENABLE
CPU FAILURE DETECT 9602
1 HZ STROBE FROM CPU
NOISE FIGURE TEST CONTROL (3)
RF KEYLINE
RECEIVER TEST STATUS
TEST XMTR STATUS
RECEIVER TEST ANTENNA SELECT (3)
RECEIVER TEST CONTROL (2)
TEST XMTR CONTROL (2)
RECEIVED RF SELECT (3)
TRANSMITTED RF SELECT (3)
55A IF SELECT (3)
RECEIVER TEST ANTENNA SELECT (3)
RECEIVER TEST ATTENUATION SELECT (8)
KEYLINE STATUS
REVISION LTR
DATE
DRAWN BY
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DEPARTMENT OF THE NAVY
SATELLITE COMMUNICATIONS LABORATORY
NAVAL POSTGRADUATE SCHOOL
MONTEREY CALIFORNIA
CONTROL MOTHERBOARD 1 BLOCK DIAGRAM AND SCHEMATIC
DRAWING NUMBER TUI-C-10
SHEET 1 OF 3

FIGURE 3.2

diagram is in Figure A.4, Sheet 1, Appendix A. The control signals from CBL12 enter CMB-I at TUI-J8, pins 35, 37 and 39. The control signal is an active LOW signal. It is first logically OR'ed in U3, 7432 with the normally low CPU TIMEOUT signal. CPU TIMEOUT is explained in Section IV.A.4; at this point it is only necessary to understand that CPU TIMEOUT is a normally-low enable signal that prevents unplanned activation of the Noise Temperature Test. The result of the logical OR of CPU TIMEOUT with one of three Noise Temperature control lines is applied to pin 6 of K1, K2 or K3 (for antenna 1, 2 or 3 respectively). A TTL LOW at pin 6 activates the relay. So if either the enable line is high or the control line is high, the relay is off. If both lines are low, 28 VDC is connected from pin 14 to pin 8 of the relay and from here routed as shown in Figure 3.1.

In the communication station, Antennas 1 and 2 are station assets, while Antenna 3 is devoted strictly to the SSA. Thus, it is sometimes desirable and quite possible for the operator to turn off power to Antenna 3 for maintenance or troubleshooting. If all power is said to be off, a worker might inadvertently short out the power supply line to the noise generator, if this line were activated. For this reason, the 28VDC (switched) line to Antenna 3 passes through a second relay located on the WSC-3 panel (WP). This relay, WP K1, a Potter

and Brumfield KRP11DB, is energized by the same power supply that feeds Antenna 3. Thus, if the power to Antenna 3 is on, the Noise Temperature test is enabled. If power to Antenna 3 is off, the required 28 VDC signal cannot reach the noise generator. See Figure A.10, Sheet 4, Appendix A.

C. TEST AND APPLICATION

The Noise Temperature Section is most easily tested by energizing each of the noise generators in turn while observing the appropriate RF or IF output on the TEST UNIT's spectrum analyzer. A Y-factor in the range of 4 to 9 dB should be observed. If not, refer to the detailed test procedures in Appendix C.

The Noise Temperature Section may be utilized in either a manual or an automatic mode. In the manual mode, the operator selects the desired antenna and activates the noise generator via the Touch Panel. With the TEST UNIT's spectrum analyzer tuned to 67 MHz for IF or 247 MHz for RF (the center of the noise generator's band pass filter), the operator observes the Y-factor and enters this number in the CPU. The computer then calculates system operating temperature and displays it on the printer-keyboard.

In the automatic mode, the computer energizes the noise generators, the array processor measures the resulting Y-factor, and then the CPU calculates and

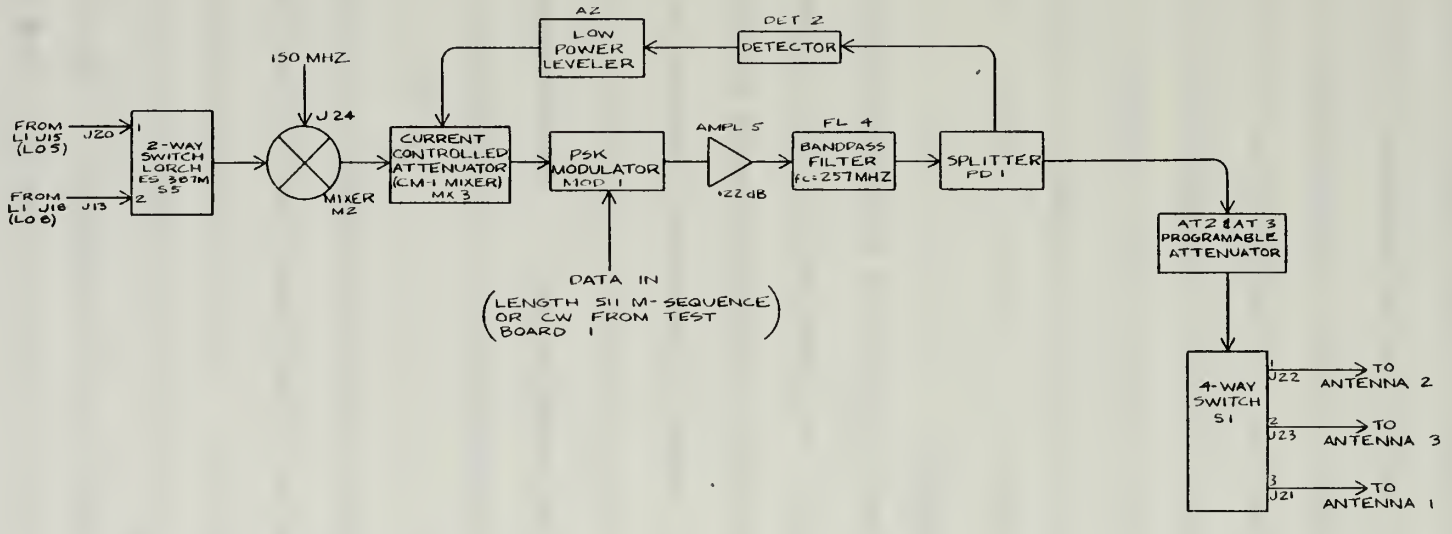
displays operating temperature. This process is repeated for each of the antennas. It should be pointed out that in the automatic mode, the Y-factor can be sensed only at the output of the RF units, whereas in the manual mode, operating temperature can be measured through RF input or output. See Figure A.10, Sheet 4 in Appendix A for a schematic diagram. Appendix G contains a set of copies of the displays observed by the operator on the TOUCH PANEL during conduct of Operating Temperature Tests.

IV. RECEIVER TEST SECTION

Required of the SSA is the capability to conduct self-tests and calibrations with the use of intrinsic equipment. The TEST UNIT provides this capability via the Receiver Test Section. A CW or PSK modulated signal of precise power level is generated in the range of 240 to 270 MHz. This signal is then coupled into the preamplifier associated with the antenna selected by the operator. See Fig. 4.1. This precisely defined signal is then available for reception at the SSA Spectrum Receivers, Frequency Receivers and the AN/WSC-3.

A. DESIGN

Figure 4.1 is a block diagram of the Receiver Test Section. The output of the local oscillator shown in the block diagram is mixed in MX2 with a 150 MHz signal from the SSA Frequency Generator to provide a signal in the range of 240 to 270 MHz. The resulting RF signal is applied to a Minicircuits Lab PAS-1 electronic attenuator, MX1. The PAS-1 is utilized as a current-controlled attenuator and is part of the Low Power Leveler discussed later. The output of the PAS-1 passes through a PSK modulator, MOD1, resulting in either a CW or PSK modulated signal, depending on the input to the modulator. This signal is band-pass filtered, (FL4), then divided in halves



TEST UNIT RF PANEL (TR)

BLOCK DIAGRAM
RECEIVER TEST SECTION

REVISION LTR		DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY
A	DATE 5/1/83	NAVAL POSTGRADUATE SCHOOL
	DATE	MONTEREY CALIFORNIA
	DATE	
	DATE	TEST UNIT RF PANEL (TR) BLOCK DIAGRAM AND SCHEMATIC
	DATE	
DRAWN BY LS	DATE 3/22/83	DRAWING NUMBER TR-C-00 — SHEET 2 OF 4
APPROVED BY	DATE	

FIGURE 4.1

(PD1). One half is applied to a diode detector, DET1 and the Low Power Leveler. The other half of the signal power goes to a Lorch electronic switch, S1, for routing to the antennas. Prior to routing to an antenna, the signal is attenuated using a pair of Daico programmable attenuators (AT2 and AT3). The output of the leveler is 0 dBm, much too high for any input to the RF preamplifier, even considering the cable and coupling loss involved. Thus, the programmable attenuators add attenuation resulting in a signal of desired level.

1. Modulation Modes

Three modes of modulation are available for Receiver Test signals: CW, PSK with data generated on Test Board I, and PSK with data generated by the HP1645A Data Error Analyzer. The latter data source is made available only for troubleshooting purposes; the normal source of data for PSK modulation is a pseudorandom sequence generator on Test Board 1. See Figure A.1, Sheet 1, Appendix A.

The pseudorandom sequence generator is of length 511 ($2^9 - 1$) and generates the same length 511 sequence provided by the HP1645A. U7, a 74164 serial in, parallel out shift register and U6 a 7474 D flip-flop are configured as a nine-stage feedback shift register. Their clock is derived from a 19.2 kHz crystal oscillator, U1, whose output is successively divided down by a series of D

flip-flops (U2 - U5). Three bits from Control Bus Latch Board 12 (CBL12) control the clock rate used for PSK modulation. These three lines are the select lines for U9, an eight-channel multiplexor whose inputs are the various clock rates from the crystal oscillator and flip-flops. A three-bit code selects one of the channels and the resulting clock rate is applied to the feedback shift register. "In order to prevent the MLS from sequencing into the all-zeros state, a comparison of each parallel output of the 74164-U7 and the output of U6-7474 PIN 9 is made. All of these are NOR'ed together in U8-74260 and then NAND'ed and tied to the set input of U6-7474 PIN 10. If the clock is low and the all zeros state is observed, the set line is brought low to change the output of U6 PIN 9 to a high value and restart the sequence." [Ref. 1]

Shown in Figure 4.2 is a schematic diagram of the logic used to select among the three modulation modes. Input lines b_1 and b_2 are control bits from CBL12. A complete list of the functions of all the bits of CBL12 and a discussion of its use is given in Appendix B. If b_1 is in the low state (0 volts), the output of U12-3 is in the high state (5 volts) regardless of the other input to this gate. If b_1 is high, the output of U12-3 will be the complement of the wired-OR combination of U12-1 and U12-2. b_2 selects between internally generated data

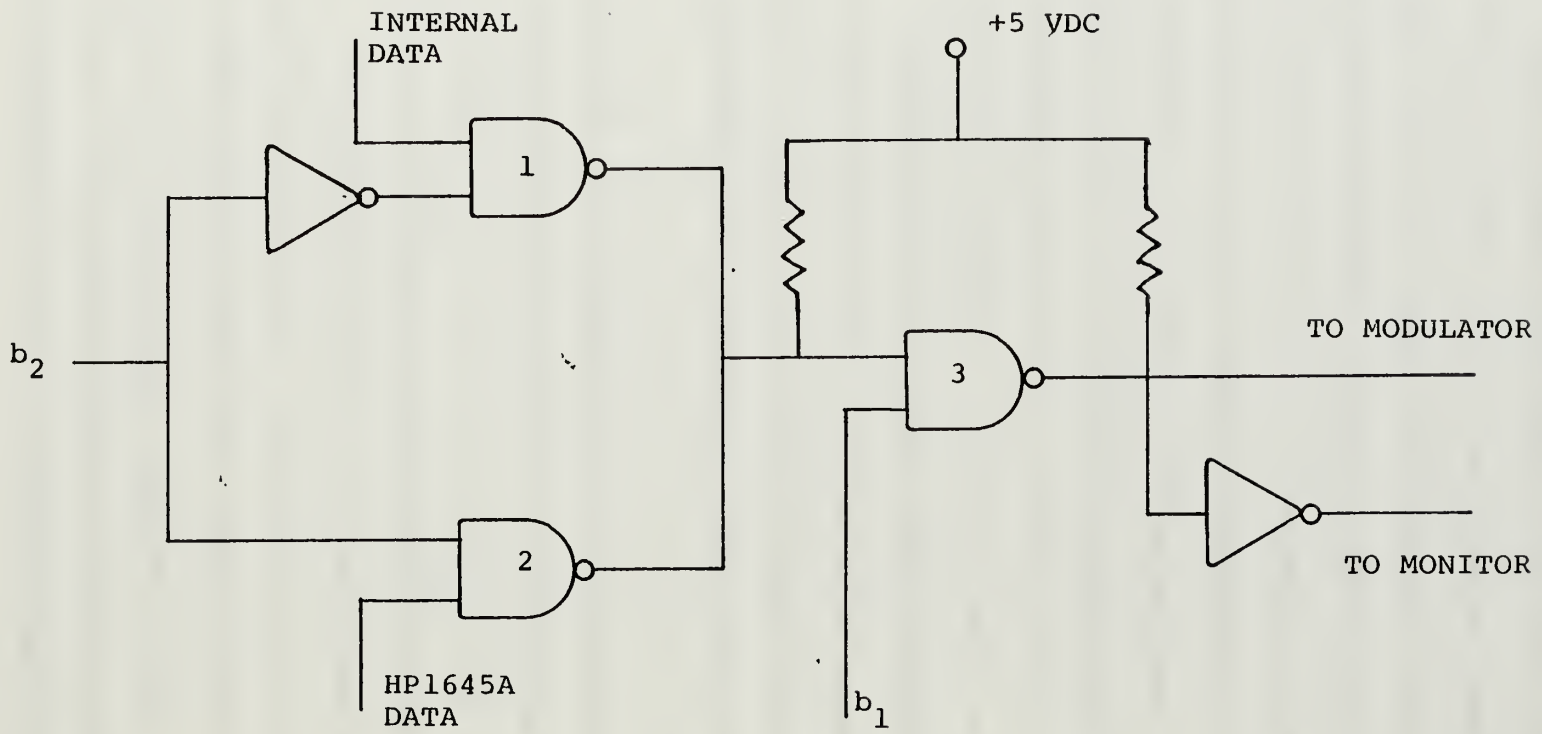

INTERNAL
DATA
+5 VDC
1
b_2
3
TO MODULATOR
2
TO MONITOR
HP1645A
DATA
b_1

FIGURE 4.2

and the HP1645A. If b_2 is high, a low level results at one input to U12-1 thus inhibiting the other input, the internal data. A high level is present at one input to U12-2, so the output of the wired-OR combination is the complement of the data from the HP1645A. If b_2 is low, the opposite result occurs. Table 4.1 summarizes the selection of one of the three possible modes.

b_1	b_2	modulation mode
0	X	CW
1	1	HP1645 data for PSK
1	0	Internal data for PSK

Table 4.1

The selected output is routed to the data input of the PSK modulator in the Receiver Test Section. It is also buffered with a 7404 inverter and routed to the Data Interface Section via Control Motherboard I.

2. Local Oscillator

The local oscillator signal present at MX2 in Figure 4.1 is provided by one of two Rockland 5610A frequency synthesizers. The 5610A is BCD programmable, with frequency resolution to ten Hertz and output level of +13 dBm. The SSA contains eight such units; L01 through L04 are devoted to Spectrum Receiver 1 through 4

respectively, L05 is shared by the Receiver Test section and the AN/WSC-3 of the TEST UNIT, L06 and L07 are devoted to the Frequency Receivers and L08 is shared by the Frequency Receivers and Receiver Test sections of the TEST UNIT.

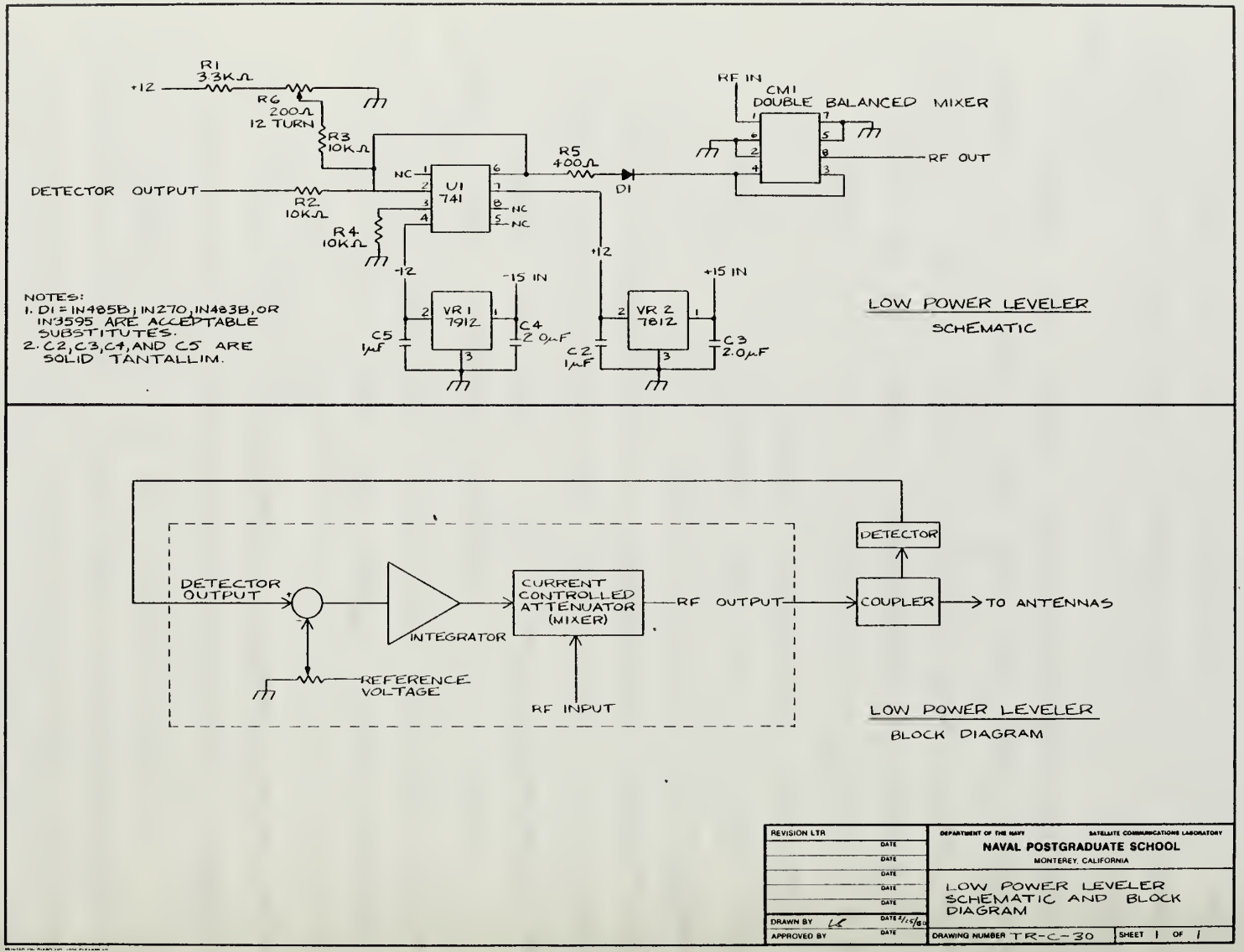
To generate Receiver Test signals, the operator chooses a frequency in the range of 240 to 270 MHz. The CPU determines which of the local oscillators shared by the Receiver Test section is available and programs that local oscillator to provide a signal in the range of 90 to 120 MHz, that when mixed with 150 MHz results in the correct frequency. Further, the computer provides a control signal via CBL12 to Lorch 2-way switch, S5, which selects the available local oscillator. This control signal enters the TEST UNIT at TUI J9, on Control Mother-board I (CMB-I). The control signal is inverted in U6; the signal and its complement are then routed to TUI J29, pins 9 and 11 respectively. These lines appear at TR J28 pins 5 and 6 where they are sent to the control pins of S5.

3. Low Power Leveler

In order to provide a signal for calibration of SSA receivers, the power level of the Receiver Test signal must be precisely controlled and virtually immune to perturbations in operating parameters. This requirement is accomplished with the Low Power Leveler. The leveler works by feeding back a portion of the Receiver Test signal,

converting RF power to a DC voltage and comparing the resulting voltage to some nominal level. If the actual output is not at the nominal level, an error voltage is produced. This error voltage is integrated in the leveler circuit and the resulting signal is applied to a current-controlled attenuator in the RF signal path. Attenuation is adjusted until the output power is back at the nominal value and the error voltage is reduced to zero. See Figure 4.1. Feedback is accomplished by splitting the output of the Receiver Test Section with the two-way power divider, PD1. One half of the power is available as a test signal. The other half is applied to a Hewlett Packard HP33330B option 003 diode detector, DET1, where the RF power is converted to a corresponding DC voltage. Table 4.2 is a table of the diode characteristics showing the relationship between output voltage and input power.

Figure 4.3 is a schematic diagram of the Low Power Leveler. The nominal level desired at the output of the leveler is 0 dBm. At 0 dBm, the output of the detector is 200 millivolts, as seen from Table 4.2. Thus, the actual detector output is summed with a nominal reference voltage of -200 millivolts at the input to U1 via R6 and R3. If an error voltage exists, U1 and C1 integrate this voltage and provide a signal to MX1, the current-controlled attenuator (Minicircuits PAS-1). The RF power cut of the PAS-1 is thus adjusted so as to reduce the resulting error


R1
3.3KΩ
+12
R6
200Ω
12 TURN
R3
10KΩ
R5
400Ω
RF IN
CM1
DOUBLE BALANCED MIXER
RF OUT
DETECTOR OUTPUT
R2
10KΩ
U1
741
NC
NC
NC
D1
R4
10KΩ
-12
-15 IN
+12
+15 IN
VR 1
7912
VR 2
7812
C5
1μF
C4
2.0μF
C2
1μF
C3
2.0μF
NOTES:
1. D1 = IN485B, IN270, IN483B, OR IN3595 ARE ACCEPTABLE SUBSTITUTES.
2. C2, C3, C4, AND C5 ARE SOLID TANTALLIM.
LOW POWER LEVELER
SCHEMATIC
DETECTOR
DETECTOR OUTPUT
INTEGRATOR
CURRENT CONTROLLED ATTENUATOR (MIXER)
RF OUTPUT
COUPLER
TO ANTENNAS
REFERENCE VOLTAGE
RF INPUT
LOW POWER LEVELER
BLOCK DIAGRAM
REVISION LTR
DATE
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DEPARTMENT OF THE NAVY
SATELLITE COMMUNICATIONS LABORATORY
NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA
LOW POWER LEVELER SCHEMATIC AND BLOCK DIAGRAM
DRAWING NUMBER TR-C-30
SHEET 1 OF 1

FIGURE 4.3

Table 4.2

DETECTOR OUTPUT FOR GIVEN INPUT POWER

From Hewlett-Packard Technical Data Sheet for HP3330B opt 003, 1 SEPT 1976.

INPUT POWER (dBm)	V_{out}
-30	500 uV
-25	2 mV
-20	5 mV
-15	15 mV
-10	40 mV
-5	100 mV
0	200 mV
5	400 mV
10	1.5 V
15	2.0 V
20	2.5 V

voltage to zero. Resistor, R5 and diode, D1, control the current flow to the PAS-1. Potentiometer R6 is used to adjust the reference voltage with which the detector output is compared. It is adjusted at calibration time to set the leveler output to 0 dBm.

4. Control

Before a Receiver Test signal is generated and injected in one of the antenna preamplifiers, three events must occur. First, the CPU must enable the test signal via CBL12; second, the operator must enable the test signal via the RCVR ENABLE pushbutton on the TEST UNIT panel; finally, the test signal is keyed on and off by the CPU via CBL12. This sequence prevents the inadvertent generation of a test signal that might be a source of confusion on the operator's part. The logic supporting this sequence is located on TEST BOARD II. See Figure A.2, Sheet 4, Appendix A. The Receiver Test enable bit from CBL12 goes high to remove the CLEAR signal to U12, 7474 flip-flop. The manual RCVR ENABLE pushbutton is inverted in U13, then applied to the CLOCK line of U12. The output of U12 is then high, and the test signal is enabled. The output of U12 is AND'ed in U14 with the receiver test on-off control bit from CBL12. Pin 3 of U14 then is the test signal control line. This control line is AND'ed with the CPU TIMEOUT signal, discussed later, in U14. The result of this operation is next AND'ed in U11 with the

antenna selection bits from CBL12. Thus, the logical AND of the test signal control line and the selected antenna control line results in a signal that: one, is inverted then routed to an electronic switch (S1) shown in Figure 4.1, to route the test signal to the desired antenna; and two, is applied to U10, ULN2003 lamp driver, to energize the appropriate indicator lamp on the TEST UNIT panel.

The logic for the CPU TIMEOUT signal mentioned earlier is located on CONTROL MOTHERBOARD I, Figure A.4, Sheet 1, Appendix A. In the event of a CPU failure or during a power-up sequence, the state of the control bits on the SSA Control Bus is random. It is possible that these bits would be in a state that results in generation of a Receiver Test signal without the operator's intent. The CPU TIMEOUT signal is generated to prevent the unwanted generation of Receiver Test signals (as well as activation of the Noise Temperature test and/or the AN/WSC-3 transmitter). The TIMEOUT signal results from the logical OR of the output of U5, a 555 timer and a U4, a 9602 multivibrator. The 555 is designed as a power-up delay. When power is turned on, the output of the 555 goes high and remains so for one second. It then goes to a low state until power is turned off, then on again, at which time the sequence repeats. The 9602 detects the presence (or absence) of a one Hertz trigger pulse from the CPU, (CBL12, BYTE0, BIT 0; TUI J8, PW21) and retriggers each

time the pulse occurs. The $\overline{Q}$ output is OR'ed with the 555, and the 9602 is configured so its $\overline{Q}$ output will always be low if the one Hertz pulse is present. In the event of CPU failure, the trigger pulse ceases and the $\overline{Q}$ line goes high. Thus in normal operation, the inputs to U3, 7432, are low. If either input is high, the output of the OR gate (U3) goes high. This output line is used as is, or inverted as necessary, to enable or disable the Noise Temperature, Receiver Test and AN/WSC-3 control circuits.

B. MEASUREMENTS AND DATA

Figure 4.4 is a graph of leveler output versus frequency. Figure 4.5 plots leveler output power versus local oscillator input power for three frequencies. These graphs indicate that the Low Power Leveler maintains a flat output characteristic across the RF band of interest and across a wide range of input power variation.

Figure 4.6 is a graph of leveler output versus modulation frequency. This plot was obtained for ten percent amplitude modulation of the local oscillator signal. The ordinate is percent modulation of the leveler output. By observing the maximum modulation that occurs at the output, then backing down by a factor of 3 dB and noting the frequency at this point, the speed of response of the leveler may be determined. Specifically,

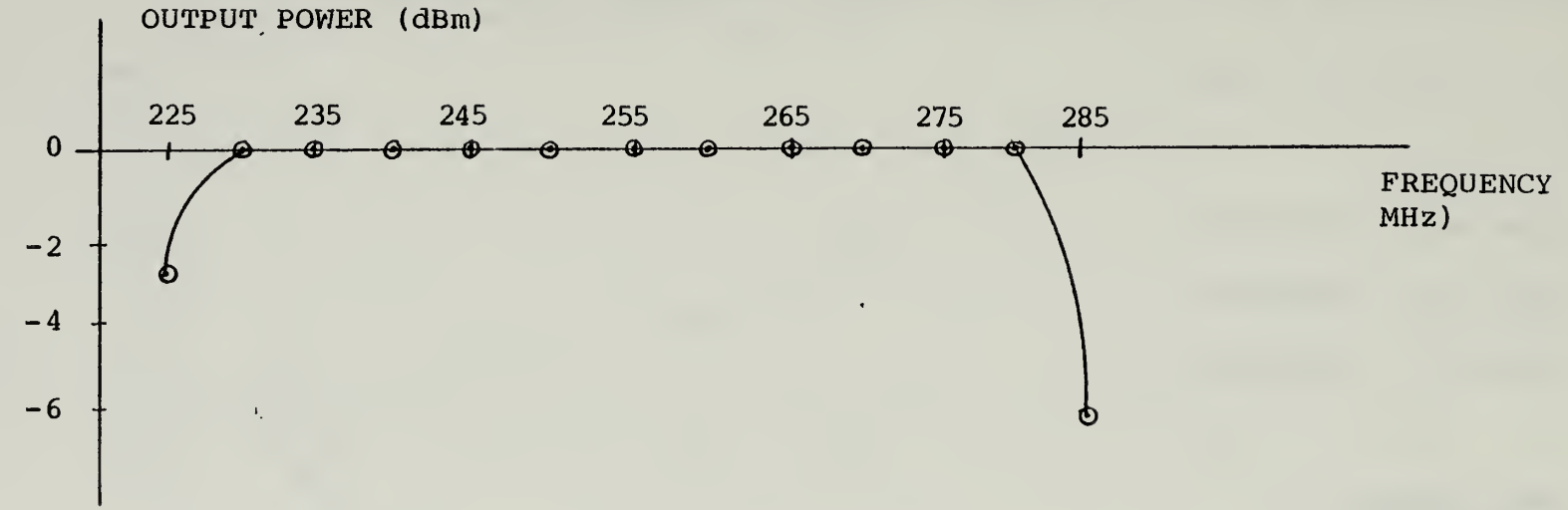


FIGURE 4.4. LOW POWER LEVELER OUTPUT VS. FREQUENCY

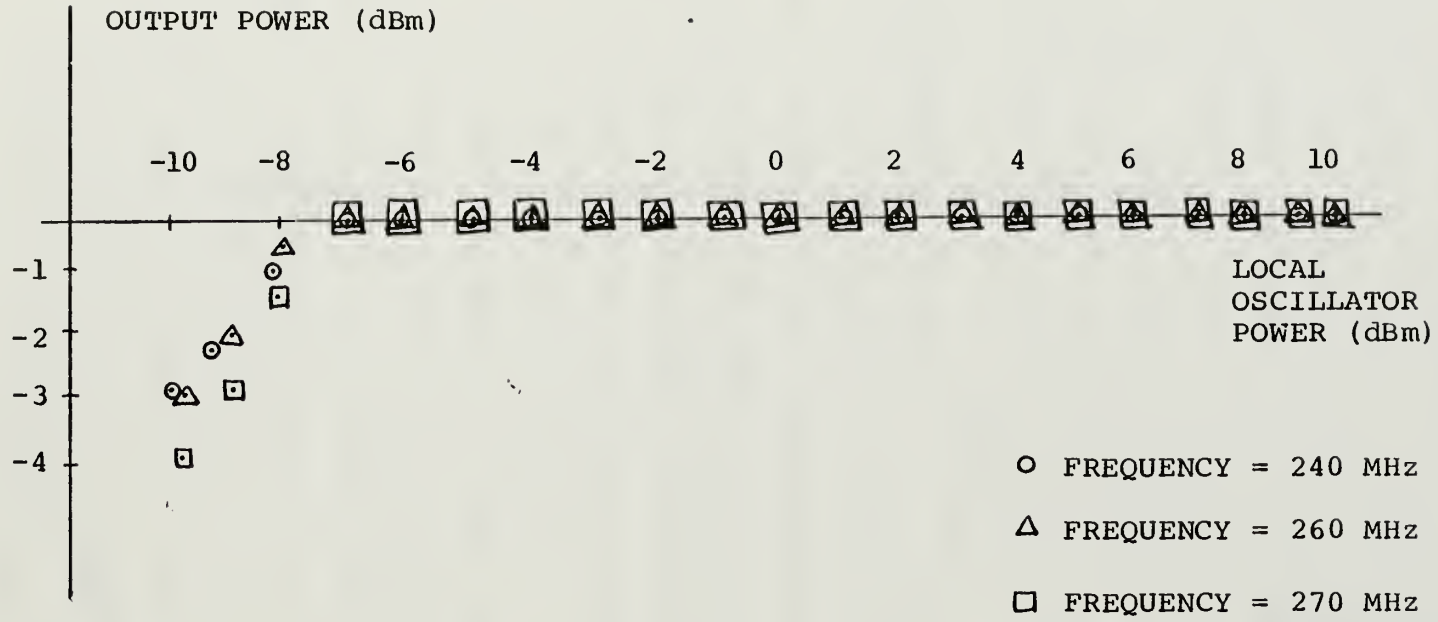


FIGURE 4.5. LOW POWER LEVELER OUTPUT VS. LOCAL OSCILLATOR POWER

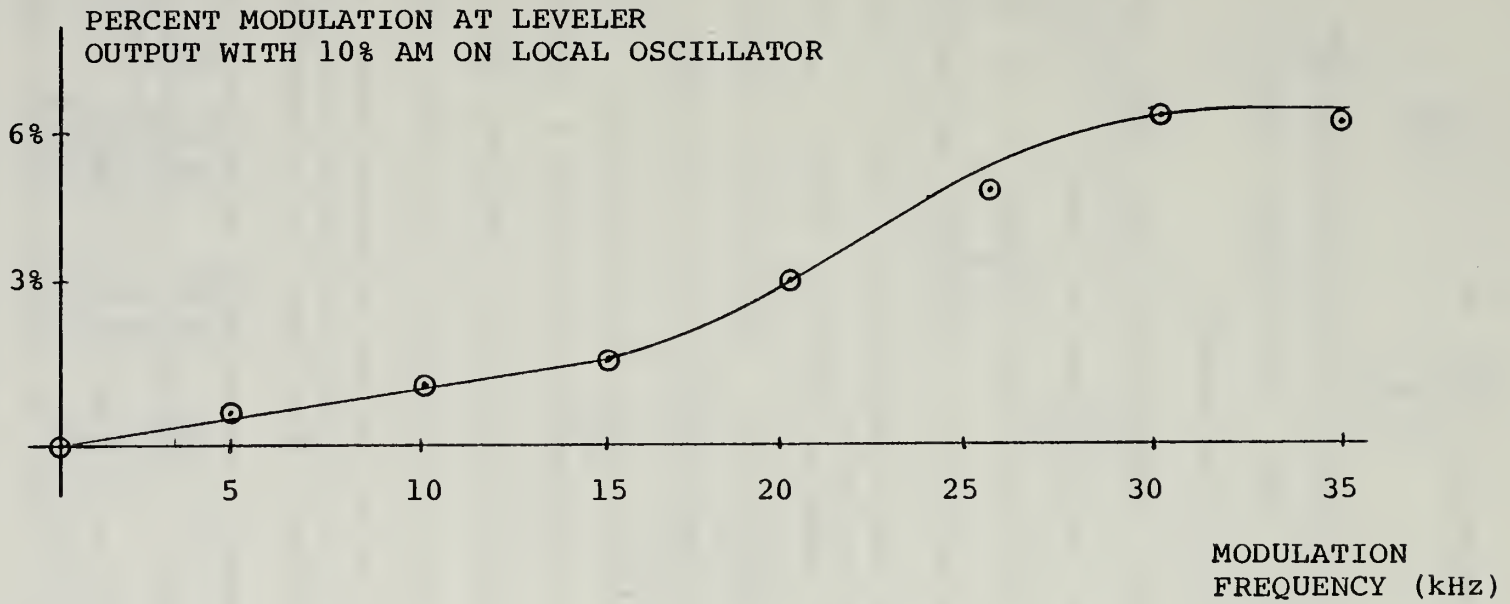


FIGURE 4.6. LOW POWER LEVELER RESPONSE TIME

$$\text{TIME CONSTANT} = \tau = \frac{1}{2\pi f_c}$$

$$\text{RESPONSE TIME} = 5\tau$$

From Figure 4.6, f_c = 25 kHz, which yields a time constant of 6.37 microseconds. Thus, the response time of the Low Power Leveler is 31.83 microseconds.

To properly employ the Receiver Test signal, the cable and coupling losses involved must be known. Figure 4.7 shows the signal flow from leveler output to the RF preamplifier in the antenna deck box. Table 4.3 tabulates the losses associated with the points labeled in Figure 4.7 for the NPS installation. (The combiner shown at point C in Figure 4.7 is discussed in Section IV.C.) Knowing the leveler output power and the total loss involved with the chosen antenna, any lower desired signal level may be applied. The cable and coupling loss is applied to the CPU as a calibration factor. When the operator applies a Receiver Test signal, the desired power level is applied to the CPU. The CPU calculates the difference between selected power and the calibration factor; this is the amount of attenuation required of the Daico programmable attenuators shown in Figure 4.7 and Figure A.9, Sheet 2, Appendix A. Attenuation control is provided by CBL12 as indicated in Appendix B.

One adjustment is required for the Receiver Test Section. At calibration time, a power meter is attached to the output

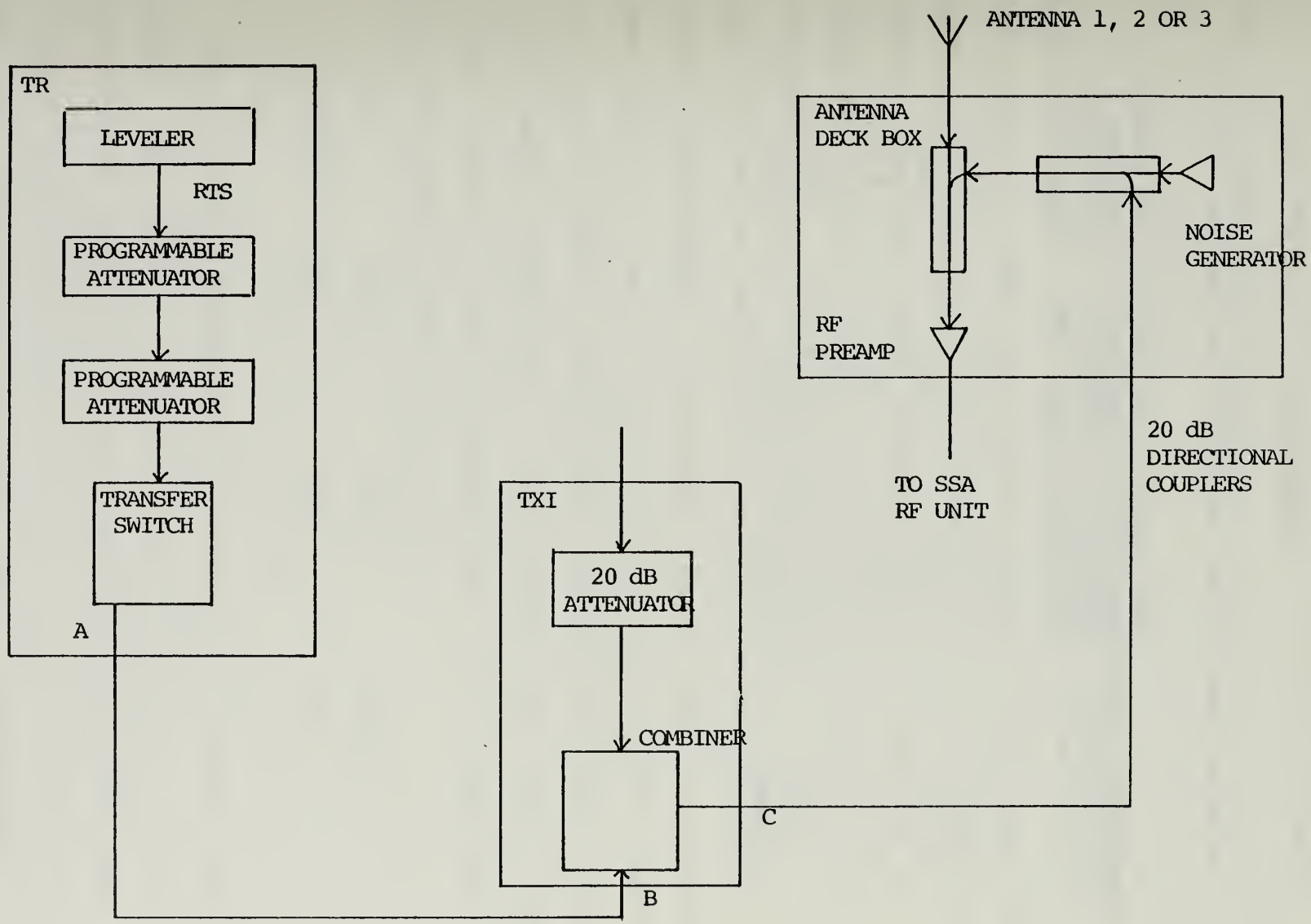

ANTENNA 1, 2 OR 3
TR
LEVELER
RTS
PROGRAMMABLE ATTENUATOR
PROGRAMMABLE ATTENUATOR
TRANSFER SWITCH
A
ANTENNA DECK BOX
NOISE GENERATOR
RF PREAMP
TO SSA RF UNIT
20 dB DIRECTIONAL COUPLERS
TXI
20 dB ATTENUATOR
COMBINER
C
B

FIGURE 4.7

TABLE 4.3

Receiver Test Signal Cable/Coupling Loss at 260 MHz

REFERENCE POINT	TEST SIGNAL ANTENNA 1 Cumulative Loss (dB)	TEST SIGNAL ANTENNA 2 Cumulative Loss (dB)	TEST SIGNAL ANTENNA 3 Cumulative Loss (dB)
Pt. A	4.3	4.3	4.3
Pt. B	5.1	5.1	5.1
Pt. C	8.3	8.3	8.4
Pt. D	21.5	20.9	20.8
Preamp.	62.1	60.4	61.3

of the power divider in the Low Power Leveler. Potentiometer R6, in the leveler circuit (Figure 4.3) is adjusted until the power meter reads 0 dBm.

C. TEST AND APPLICATION

The Receiver Test Section may be tested by generating a signal of desired level and frequency at a chosen antenna, then tuning the TEST UNIT spectrum analyzer to the same frequency and selecting the appropriate signal on the TEST UNIT panel. Frequency, power level and modulation may then be verified. Shown in Figure 4.7 is a combiner on TXI in the RF signal path of the Receiver Test Section. A signal generator may be used to inject a signal at the available port of the combiner. This signal may be used as a Receiver Test signal in case of a failure of the Receiver Test Section, or it may be used to trouble-shoot the Receiver Test Section as discussed in Appendix C. The loss from the input of the 20 dB attenuator to the RF preamplifier has been measured as follows for the NPS installation:

JACK:	TXI-J1	TXI-J2	TXI-J3
ANTENNA:	ANT 1	ANT 2	ANT 3
LOSS:	77 dB	75.2 dB	76 dB

Receiver Test signals may be used for two primary functions. The first is to verify correct operation of SSA receivers by generating a test signal and recovering the signal with the receiver in question. The second is to calibrate SSA Spectrum Receivers. This is accomplished by

generating test signals at various frequencies across the pass-band. These signals are recovered by the Spectrum Receiver and the output observed. The output will likely be different for different frequencies. The variation in receiver output power is then used to adjust measurements made during actual spectrum analysis so that the Spectrum Receiver appears to have a perfectly flat filter characteristic. Appendix G contains a set of displays seen by the operator on the SSA Touch Panel during use of Receiver Test signals. Also included is a set of associated instructions. These displays and instructions document the specific applications of the Receiver Test Section.

V. AN/WSC-3 SECTION

Required of the SSA are the capabilities to generate uplink signals, perform power balancing, and receive and demodulate AM or FM signals. An AN/WSC-3 Satellite Communications Transceiver is employed and provides these capabilities as well as PSK and FSK demodulation. As designed, the AN/WSC-3 is under complete control of the SSA and its CPU; once initial set-up is accomplished the operator need not adjust the AN/WSC-3. If desired, however, the AN/WSC-3 may be freed of SSA control and operated manually.

A. DESIGN

A concise list of AN/WSC-3 operating characteristics is provided in Table 5.1. The AN/WSC-3 was developed to operate in the local mode, using the controls on its front panel, or in the remote mode, using a remote control box connected to the AN/WSC-3 via a pair of jacks at the rear of the transceiver. The SSA controls the AN/WSC-3 by placing it in the remote mode and replacing the remote control box with signals generated by the TEST UNIT and the SSA Control Bus. In addition to substituting the TEST UNIT for the remote control box, several modifications to AN/WSC-3 circuits were required. These modifications included alteration of AN/WSC-3 receive circuits to

TABLE 5.1

AN/WSC-3 Operating Characteristics (From Reference 2)

CHARACTERISTIC	SPECIFICATION
PRINCIPAL CHARACTERISTICS	
Frequency range	225.00 to 399.975 MHz
Number of Channels	7,000
Channel spacing	25 kHz
Preset Channels	20
Transmitter power output:	
FM and data	100 watts
AM	30 watts
SATCOM receiver offset	Provides up to six receiver offset frequencies
Transmitter	
VSWR	Will operate in a VSWR up to 2.5:1. Protected for a VSWR greater than 4:1.
Harmonic attenuation	Attenuated to 60 dB, minimum, below full power output
AM harmonic distortion	Less than 5 percent at 90 percent modulation
FM voice modulation	16-kHz P-P deviation causes 100-percent modulation
Receiver	
Selectivity	±15 kHz, minimum, 3 dB; ±50 kHz, maximum, 60 dB

TABLE 5.1 (Cont'd)

Sensitivity:	
AM	3.5 microvolts (open circuit) for S+N/N ratio ≥10 dB at 30 percent modulation at 1000 Hz.
FM	3.0 microvolts (open circuit) for S+N/N ratio ≥10 dB modulated ±2500 Hz at 1000 Hz.
Spurious response	100 dB below desired signal
AM harmonic distortion	Less than 5 percent
Pulse blanking	In-band, radar-type interference blanking circuit incorporated
Modem Performance	
Modulation/demodulation signal inputs/outputs	75-B/S, teletype, 75, 300, 1200, 2400, 4800, and 9600 B/S PSK-digital data, audio
Modem carrier frequency	70 MHz
AM carrier noise level	40 dB below a 90-percent modulated carrier
AM modulation	A 0-dBm input signal between 300 and 3500 Hz results in carrier modulation of at least 95 percent
FSK data frequency acquisition	±500 Hz minimum for 75 BAUD

TABLE 5.1 (Cont'd)

External Modem Interface

Inputs to Radio Set:	
Frequency	70 MHz
3-dB bandwidth	±250 kHz
Power level	0 dBm ±1 dB
Impedance	50 ohms
VSWR	1.5:1, maximum
Outputs from Radio Set:	
Frequency	70 MHz
3-dB bandwidth	±250 kHz
Load Impedance	50 ohms
Load VSWR	1.5:1, maximum

avoid conflict with the external modem, automatic selection of external modem, provision for automatic frequency selection and provision for SSA control of transmit power level.

1. Modification to the AN/WSC-3

a. Modification Control

Normally, the AN/WSC-3 is used under SSA control, and the modifications listed above must be implemented. There are occasions, however, when the AN/WSC-3 is freed from SSA control and the transceiver must be returned to its normal configuration. To use the AN/WSC-3 under SSA control, the following settings are made on its front panel: the REMOTE-LOCAL switch is set to REMOTE; the FREQUENCY SELECT swtich is set to PRESET; the SATCOM-LOS switch is set to LOS. The REMOTE-LOCAL switch controls a relay that has been installed within the AN/WSC-3. When REMOTE is selected, those modifications involving external modem selection and transmit power control are implemented. When LOCAL is selected, these modifications are removed and the AN/WSC-3 responds to commands from its front panel. Additionally, this relay may be disabled, thus returning the AN/WSC-3 to a completely unmodified state. Figure A.11, Appendix A shows a schematic diagram of the relay that controls AN/WSC-3 modifications.

b. Modifications to Receive Circuits

Normal operation of the AN/WSC-3 within the SSA calls for use of an external modem for transmitting, while using internal circuits for signal reception. The AN/WSC-3 was designed for use with either external modem or internal circuits but not both simultaneously. The reason for this is that the presence of an external modem signal inhibits data recovery in PSK and FSK receive circuits due to crosstalk within the transceiver. Thus, an external modem was intended to be used both for transmitting and receiving or not at all. As discussed in paragraph 1 above, selection of REMOTE results in selection of the "external modem" position of the modulation select switch on the AN/WSC-3 front panel. Thus, since the SSA controls the AN/WSC-3 in the REMOTE mode, the external modem selection is always made. Selection of this switch position results in a disable signal present at modules 1A1A15, AM DETECTOR, and 1A1A19, DATA BUFFER, within the AN/WSC-3. In order to prevent the disabling of these modules when "external modem" is selected, these disable lines are physically cut and brought out to a switch installed in the AN/WSC-3. This switch is the same one used to enable or disable the AN/WSC-3 modifications. See Figure A.11, Appendix A. Whenever the AN/WSC modifications are in effect, the disable lines from the "external modem" switch position are removed from modules 1A1A15

and 1A1A19. Thus, under SSA control, the external modem is enabled for transmit functions as required, but selection of external modem does not disable AN/WSC-3 receive circuits. If the AN/WSC-3 modification is disabled and the transceiver is operated manually, the disable lines to 1A1A15 and 1A1A19 are returned to their normal configuration. If the operator then manually selects "external modem" on the modulation switch; an external modem must be provided for both transmit and receive functions as some AN/WSC-3 receive circuits will be disabled by this selection.

c. Automatic Frequency Selection

Normal frequency selection within the AN/WSC-3 is made via a set of thumbwheels on the transceiver's front panel or by selection of one of twenty preset channels. A frequency select switch is also located on the front panel that is positioned to choose between manual (thumbwheel) or preset frequency control. (Under SSA operation, PRESET is normally selected.) The AN/WSC-3 preset frequency programming module is accessed from the front panel. It contains twenty sets of switches, programmed by the operator, that establish twenty BCD frequency select codes. Thus, frequency control circuits within the AN/WSC-3 look for a BCD code from either the thumbwheels or the preset frequency module. One of these two sources is selected by the MANUAL-PRESET switch on the

front panel. In the REMOTE mode, PRESET is always selected and the remote control box provides a 5-bit code that selects one of the twenty preset frequencies.

The SSA seeks to automate the use of the AN/WSC-3, so that the operator may control all functions from his console. Thus, it is not desirable for the operator to dial a set of thumbwheels each time he wishes to make a change of frequency. On the other hand, the choice of only twenty preset frequencies is not satisfactory for the diversity of SSA applications. The solution to the frequency control problem is a modification to the preset channel assembly. The unmodified preset channel assembly provides 15 bits of BCD code to the pins of its connector, organized as shown in Table 5.2. Further, this module provides a jumper between pins 26 and 27 that acts as a keyline interlock. The preset channel assembly has been modified by replacing all of its circuits with a 27-lead cable. Nineteen of these leads are soldered to the connector. Of these 19 leads, 15 are connected to the original BCD frequency control pins. One is connected to a ground pin. The other three are connected to three previously unused pins and are used for the power control modification discussed later. Finally, a jumper is connected between pins 26 and 27. The other end of the cable is routed to the WP panel of the TEST UNIT. See Figure A.10, Sheet 2, Appendix A.

TABLE 5.2

FREQUENCY	BCD WEIGHT	PIN
25 kHz	1	24
25 kHz	2	23
100 kHz	8	22
100 kHz	4	21
100 kHz	2	20
100 kHz	1	19
1 MHz	8	18
1 MHz	4	17
1 MHz	2	16
1 MHz	1	15
10 MHz	8	14
10 MHz	4	13
10 MHz	2	12
10 MHz	1	11
200/300 MHz*	-	10

*H = 200 MHz
L = 300 MHz

The 15 BCD frequency control lines are routed to the Test Transmitter board where they are mated with CBL11. See Figure A.3, Sheet 4, Appendix A. During SSA operation, AN/WSC-3 frequency is selected at the operator's console, via the Touch Panel. The SSA's CPU then converts the selected frequency to a BCD code which is latched on CBL11. This BCD code is then routed to the AN/WSC-3 via the TEST XMTR board and the preset frequency modification. The AN/WSC-3 then performs as if it had received a BCD code from its normal preset channel assembly. If manual frequency control is used, as is the case during operation in the LOCAL mode, the 15 frequency control lines of CBL11 must all be set to the HIGH state. Failure to do so results in an ambiguous frequency command to the AN/WSC-3.

d. Transmit Power Control

The AN/WSC-3 is capable of transmitting signals in the range of 0 dBW to 20 dBW. As originally designed, output power level was controlled manually via the RF power potentiometer located on the transceiver's front panel. The voltage at the wiper of this potentiometer varies between about 0.5 VDC and 2.8 VDC. The voltage selected on the potentiometer wiper is then routed to power control circuits within the AN/WSC-3.

During normal SSA operation, it is required that the operator is able to control the AN/WSC-3 from

the Touch Panel; this includes output power level control. The AN/WSC-3 has been modified so that under SSA remote operation, the power control potentiometer is replaced with an automatic power control potentiometer is replaced with an automatic power control circuit in the TEST UNIT. When the AN/WSC-3 is freed of SSA control, the potentiometer on the front panel is returned to the original configuration. See Figure A-11, Appendix A. The relay is a Teledyne 732 TN-5. Power to the relay is routed via one pole of the 3PDT switch shown in the figure. This switch allows the relay to be enabled or disabled; the relay is enabled to SSA operation and disabled if the AN/WSC-3 is to be operated manually.

When the relay is enabled and the AN/WSC-3 REMOTE-LOCAL switch is in the REMOTE position, the relay is switched. When this occurs, the power circuits of the AN/WSC-3 receive power control voltages from the High Power Leveler of the TEST UNIT. When the relay is disabled or the REMOTE-LOCAL switch is in the LOCAL position, the power control potentiometer is connected to AN/WSC-3 power circuits.

In addition to installation of the relay and switch, two wires are routed from the TEST UNIT, external to the AN/WSC-3, to within the transceiver, behind the front panel. These wires come in to the AN/WSC-3 via the frequency select cable and are connected to pins 36 and 37 (previously unused) of 1A1A120 P1. Two wires are then connected from the corresponding pins on the mating jack within the AN/WSC-3

to appropriate points behind the front panel. Pin 36 is connected to the low voltage end (terminal 3) of the power control potentiometer. This line is a reference voltage to the High Power Leveler. Pin 37 is connected to the relay installed within the AN/WSC-3. This second line is the output of the High Power Leveler. Operation of the High Power Leveler is discussed in a later section.

e. Summary of Modifications

This section summarizes the parts, nature and function of all modifications made to the AN/WSC-3.

(1) Parts

One Teledyne 732 TN-5 relay

One ALCO MST 305D 3PDT switch

One 1 KΩ, $\frac{1}{4}$W resistor

One ANSLEY 609-37P D-connector

(2) Teledyne Relay

One relay within the 732 TN-5 is for the power control modification. If the relay is enabled and the REMOTE-LOCAL switch is in REMOTE, power is controlled by the High Power Leveler. If the 732 TN-5 is disabled or the REMOTE-LOCAL switch is in LOCAL, power is controlled by the potentiometer on the front panel of the AN/WSC-3.

(3) ALCO Switch

Two terminals of a 3PDT switch are used. The first switches +5VDC power supply to the relay. This terminal is used to enable or disable the AN/WSC-3 modifications.

The second terminal of the 3PDT switch is used to prevent disabling of AN/WSC-3 receive circuits due to external modem selection.

(4) The following leads have been disconnected from their normal location within the AN/WSC-3 and reconnected as indicated: (See Figure A.11, Appendix A.)

WIRE/TERMINAL	NEW LOCATION
Terminal 2 (wiper) of the power control potentiometer	Normally closed relay contact (pin 4)
Power control wire from wiper to power circuits (A1A10 pin 8)	Common contact of relay (pin 2)
A1A15 pin 24 A1A19 pin 9 A1A19 pin 30	Disable modification terminal of the 3PDT switch

(5) The following wires have been added within the AN/WSC-3:

SOURCE	DESTINATION
A1S11 pin 1 (external modem position of modulation select switch)	Common contact of relay (pin 8)
A1S3 pin 7 (REMOTE-LOCAL switch)	Control line of relay (pin 10). +12 VDC at A1S3 pin 7 activates the relay.
A1S7 pin 2	"Modification enable" terminal of 3PDT switch. This is the +5VDC supply to the relay.
A1A20 P1 (preset frequency assembly) pin 37	Normally open contact (pin 3) of relay. High Power Leveler output to AN/WSC-3.

SOURCE (cont)	DESTINATION (cont)
A1A20 P1 pin 36	Terminal 3 of power control potentiometer. Reference from AN/WSC-3 to High Power Leveler.

(6) Frequency Selection

The preset frequency assembly (1A1A20) has been removed and replaced with a single cable providing fifteen lines of BCD frequency control. Table 5.2 lists pin numbers and corresponding frequency. Pins 26 and 27 of 1A1A20 P1 are jumpered.

2. AN/WSC-3 Receive

The AN/WSC-3 is capable of receiving and demodulating AM, FM, FSK, and PSK at the following rates: 75, 300, 1200, 2400, 4800 and 9600 bits per second. Table 5.1 provides information as to selectivity and sensitivity. Received SSA signals are routed to the AN/WSC-3 via the WSC-3 Panel (WP) of the TEST UNIT. WP provides frequency conversion, filtering and amplification of received signals before injecting them into the AN/WSC-3. Signals are provided at WP by the SSA's signal Selector Unit.

a. Demodulation Mode

Modulation and demodulation mode within the AN/WSC-3 may be selected manually via the Modulation Select switch on the front panel, or remotely by entering a four-bit modulation select code at RT J3 at the rear of the radio. The modulation select switch on the front panel allows selection

of AM, FM, FSK, all PSK rates and EXTERNAL MODEM. Remote selection of modulation mode provides the same capability less EXTERNAL MODEM. Under SSA operation, modulation mode is controlled remotely, with the TEST UNIT providing the required inputs to J3 of the AN/WSC-3. Since all SSA transmit operations are performed with an external modem, provision must be made to select the EXTERNAL MODEM position of the modulation select switch. That is the purpose of the modification to the AN/WSC-3 discussed in paragraph V.A.1.a. Since internal AN/WSC-3 circuits are used for signal reception, the inputs to RT J3 are used to determine the demodulation mode. Table 5.3 lists a truth table for the four-bit code and the resulting demodulation mode. Code lines A, B, C and D are input to RT J3, pins H, J, K and L respectively. These lines are included in a cable from WP J13 to RT J3. WP J13 receives demodulation codes from the Test Transmitter board.

Figure A.3, Appendix A is a schematic diagram of the Test Transmitter board. This board is mounted on WP and provides data for PSK modulation, circuitry for AN/WSC-3 power control, antenna selection logic and an interface between CBL11 and the AN/WSC-3 section of the TEST UNIT. It is this interface that is of interest in demodulation mode control. CBL11 provides a four-bit code to the Test Transmitter board. This code is based on the operator's selection of demodulation mode on the SSA Touch Panel. Each of the four control lines

TABLE 5.3

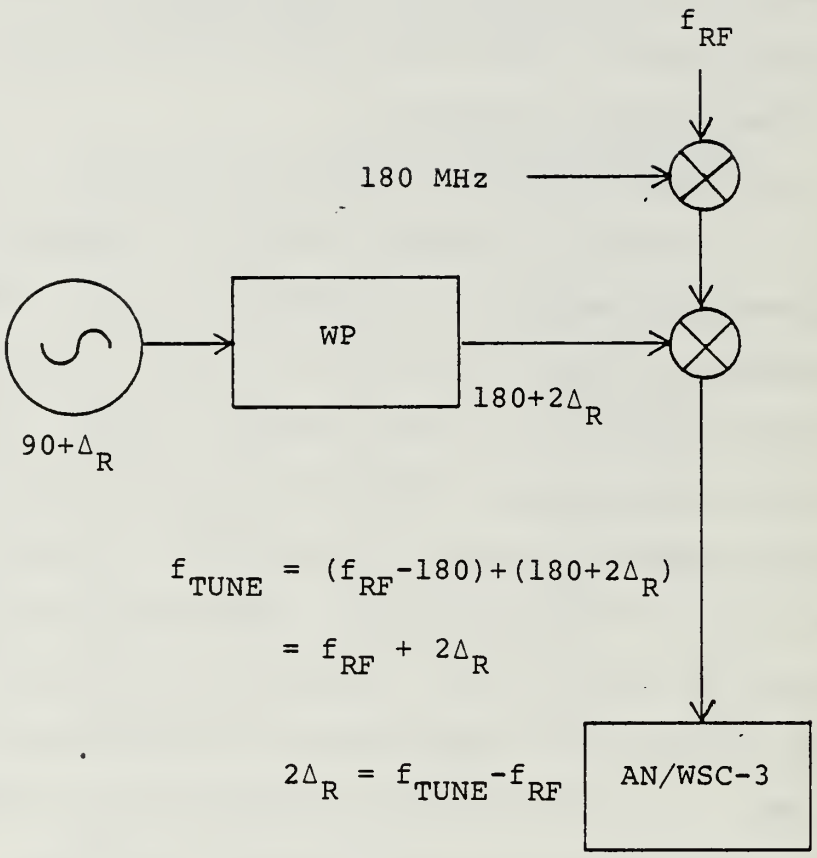
Demodulation Mode Selection

D	C	B	A	MODE SELECTED
H	H	H	H	PSK 75
H	H	H	L	PSK 300
H	H	L	H	PSK 1200
H	H	L	L	PSK 2400
H	L	H	H	PSK 4800
H	L	H	L	PSK 9600
H	L	L	H	FSK
H	L	L	L	FM
L	H	H	H	AM

is buffered in one gate of U23, 7432 quad OR gate, and then is routed to WP J13 and RT J3. The buffer is required to isolate the latch on CBL11 from the 4000 pf filters on the input lines inside the AN/WSC-3.

b. Signal Input and Frequency Control

Frequency selection within the AN/WSC-3 is accomplished as described in paragraph V.A.1.c. Note that according to Table 5.1 and 5.2, AN/WSC-3 frequency may be selected only to 25 kHz channel centers. This 25 kHz resolution is not satisfactory for SSA operation; much finer frequency control is required. To solve this problem, received SSA signals are down-converted by 180 MHz at the SSA RF Units. These IF signals are routed to WP in the TEST UNIT where they are up-converted by $180 + \Delta$ MHz. Δ is the difference between the 25 kHz channel centers and the actual desired frequency. This up-converted signal is now in the RF passband (240 - 270 MHz) and is centered on one of the 25 kHz channels of the AN/WSC-3. Figure 5.1 is a block diagram of this operation. When the operator chooses AN/WSC-3 receive operations, the receive frequency is selected via the SSA Touch Panel. The SSA CPU then calculates the parameters shown in Figure 5.1 and programs Local Oscillator 5 accordingly.



Let f_{TUNE} be f_{RF} or next highest 100 kHz frequency.

$$\Delta_R = \frac{f_{TUNE} - f_{RF}}{2}$$

Find Δ_R

PROGRAM L05 to $90+\Delta_R$ MHz.

FIGURE 5.1

Figure A.10, Sheet 1, Appendix A is a schematic diagram of the AN/WSC-3 receive section of the WSC-3 panel (WP). The local oscillator signal enters WP at WP J7. Here the signal is split via 10 dB coupler, CP1. The coupled portion goes to the external modem section of WP. The output of the coupler goes to frequency doubler, DBL1. Since the local oscillator is programmed by the CPU to 90 + $\Delta/2$ MHz, this signal frequency must be doubled, as a frequency of 180 + Δ MHz is needed. The resulting signal is amplified in AMPL1, an ANZAC AM-105, and then bandpass-filtered in FL2. Merrimac mixer, MX1 uses this signal to up-convert the SSA received signal from the Signal Selector. This RF signal is amplified once again (AMPL2) and then applied to the AN/WSC-3 receive jack, RT J9.

c. Demodulated Signals

The received and demodulated signals out of the AN/WSC-3 are of two basic types: AM or FM audio signals and PSK or FSK data. (FSK will rarely be encountered in the SSA, but the capability exists, if needed.)

(1) PSK and FSK data is recovered at RT J2, pin 67. RT J2 is connected to WP J12, and pin 67 of J2 is connected to pin 11 of J12. See Figure A.10, Sheet 1, Appendix A. From WP J12, the recovered data is routed to the Data Interface. The Data Interface is discussed in

detail in Chapter VI. In general terms, PSK and FSK data out of the AN/WSC-3 is of MIL-188 format (±6 Volts). The Data Interface converts these MIL-188 signals to TTL level signals and routes them to an output jack on the DI panel. The Data Interface also sends the MIL-188 level signal to the HP1645A Data Error Analyzer for bit error rate testing.

(2) Audio signals from the AN/WSC-3 are provided in two forms, wideband audio and narrowband audio; of interest to the SSA is narrowband audio. Pin 36 of RT J2 (connected via cable to WP J12) is connected to ground; this pin selects between wideband or narrowband, and a TTL LOW (ground) selects narrowband. The demodulated narrowband audio (AM or FM) is present at RT J3, pin m. This pin is routed via cable to WP J13, pin 13 and then to WP J4. See Figure A.10, Sheet 1, Appendix A. WP J4 is connected to the SSA AUDIO SELECTOR, AS J5. From the AUDIO SELECTOR, the received AM/FM signal may be recorded on tape, sounded over a loudspeaker or displayed on the TEST UNIT oscilloscope (see Section II.C, Time Domain Signal Display).

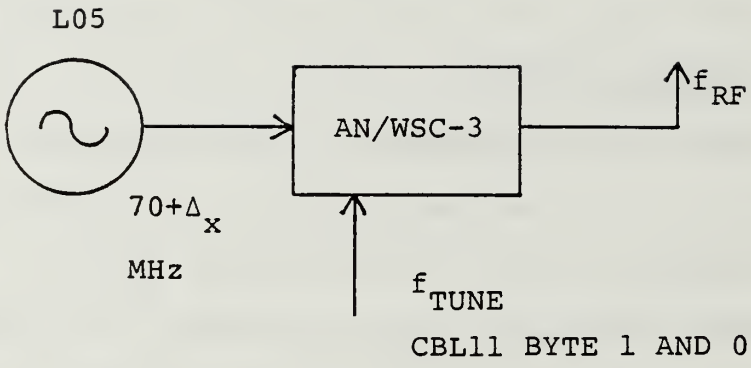
3. AN/WSC-3 Transmit

The AN/WSC-3 is used to transmit a CW signal in conjunction with power balance operations or to transmit a CW or PSK signal for general uplink operations. Provision is not made for voice or FSK data transmission

except during the LOCAL mode of operation. Design considerations include frequency selection, power control, antenna selection, and generation of an external modem signal.

a. Frequency Control

Selection of frequency within the AN/WSC-3 is accomplished via the frequency control modification discussed in Section V.A.1.C. As described in that section, AN/WSC-3 frequency may be selected only on the 25 kHz channel centers. Operation of the AN/WSC-3 within the SSA requires much finer frequency resolution. This resolution is achieved by perturbing the local oscillator used in generating the external modem signal. (Details of the external modem are discussed in Section V.A.3.c). Refer to Figure 5.2. As indicated in the figure, the local oscillator is tuned to $70 + \Delta_x$ MHz. Δ_x is the difference between the frequency selected within the AN/WSC-3 and the desired frequency of transmission. Although the AN/WSC-3 may be tuned to some multiple of 25 kHz, it is necessary only to tune the radio to the next 100 kHz frequency above the desired frequency. This is due to the wide frequency range available from the local oscillator. Also note that according to Table 5.1, the 3 dB bandwidth of the external modem is specified as ±250 kHz; thus 100 kHz deviations about 70 MHz present no



$$f_{RF} = f_{TUNE} - \Delta_x$$

$$\Delta_x = f_{TUNE} - f_{RF}$$

Let f_{TUNE} be next 100 kHZ over f_{RF}.

Find Δ_x

PROGRAM L05 to $70+\Delta_x$ MHz

FIGURE 5.2

problem. Frequency is selected by the operator via the SSA TOUCH PANEL; detailed procedures are discussed in Section V.B.

b. Power Control

AN/WSC-3 power is normally controlled from the front panel of the radio via the power control knob. This knob varies the voltage seen at the wiper of a potentiometer; the wiper voltage is routed to power control circuits within the AN/WSC-3. Under SSA control, it is required that AN/WSC-3 power be controlled from the SSA TOUCH PANEL. This feature is accomplished through use of the High Power Leveler of the TEST UNIT. Details concerning the AN/WSC-3 modification that allows external power control are covered in Section V.A.1.d. This section describes the design and functioning of the High Power Leveler.

A block diagram of the High Power Leveler is shown in Figure 5.3. The directional coupler, programmable attenuator, diode detector and momentary switch are mounted on the WSC-3 Panel (WP). The electronic circuitry shown in the figure is located on the TEST TRANSMITTER board.

The High Power Leveler operates by feeding back a portion of the transmitted RF power through the 30 dB directional coupler in Figure 5.3. The diode detector converts the fedback power to a corresponding DC voltage. This DC voltage is compared to some nominal

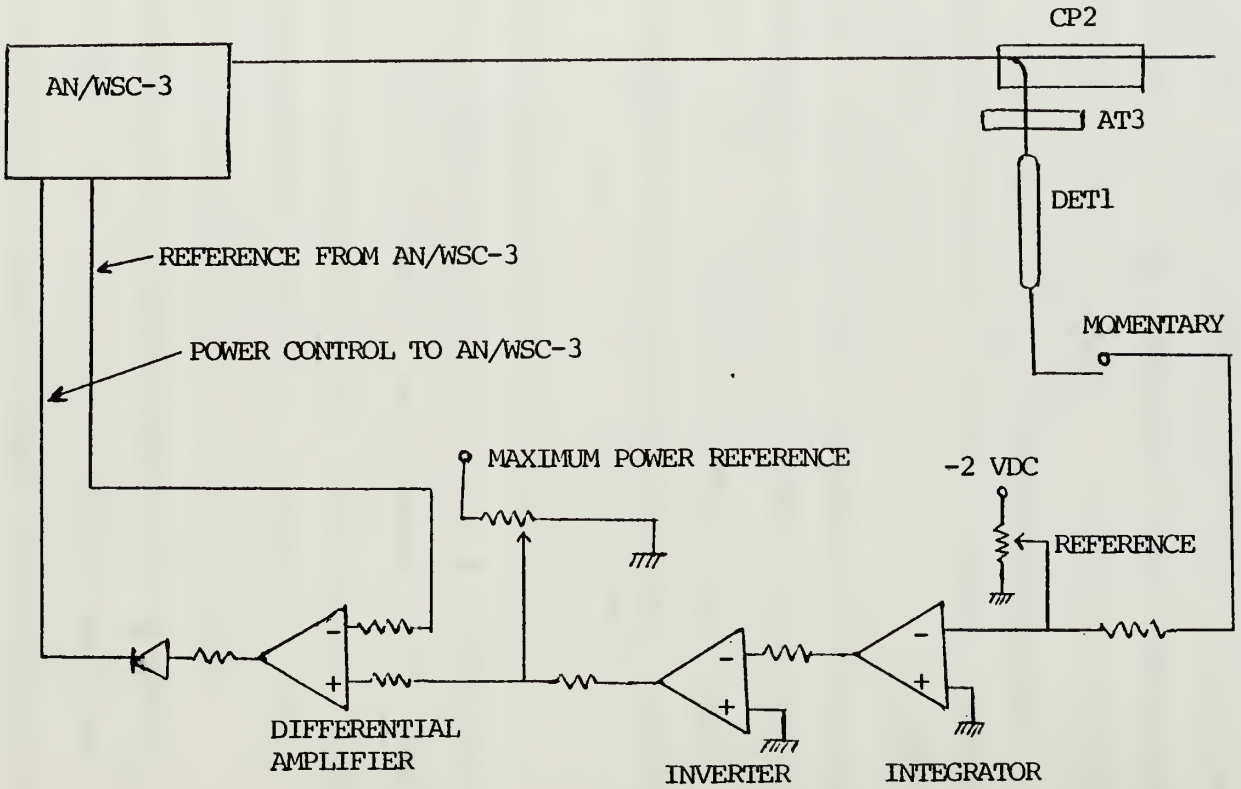

CP2
AN/WSC-3
AT3
DET1
REFERENCE FROM AN/WSC-3
POWER CONTROL TO AN/WSC-3
MOMENTARY
MAXIMUM POWER REFERENCE
-2 VDC
REFERENCE
DIFFERENTIAL AMPLIFIER
INVERTER
INTEGRATOR

FIGURE 5.3

voltage; any resulting error voltage is applied to the High Power Leveler circuit. The circuit converts the input error into a power control signal to the AN/WSC-3 which drives the transmitted RF power back to the nominal level. This principle of operation is the same as that for the Low Power Leveler. The difference lies in the programmable attenuator, AT3, between the directional coupler and the diode detector. The nominal voltage reference at the input to the leveling circuit assumes zero attenuation in the feedback path. Under such a condition, the circuit does nothing and the power out of the AN/WSC-3 is at the nominal level. Attenuating the fed-back power results in an error voltage at the input to the leveling circuit. As previously explained this error voltage results in a control signal to AN/WSC-3 power circuits. Each one-dB step of attenuation in the feedback path results in a one-dB increase in the transmitter output power.

The attenuator is a DAICO 100C1427 programmable step attenuator. It provides steps of 1, 2, 4, 8 and 16 dB, which may be combined to give any desired attenuation up to 31 dB. Control of the attenuator comes from the Test Transmitter board via WP J19. See Figure A.3, Sheet 3, Appendix A. The DAICO step attenuator operates at 28 VDC, 17 mA. Control is initiated on CBL11, and accordingly is at TTL levels. (See Appendix B for a

list of CBL11 functions.) U19 on the Test Transmitter board is used as a driver to convert the TTL power commands into a 28 VDC control signal.

The detector, DET1, shown in Figure 5.3 is a Hewlett-Packard HP33330B option 003 Schottky diode detector. Its input-output characteristic is discussed in Section IV.A.3. The DC voltage out of the detector is routed to the leveling circuit via a normally closed momentary switch, S1, and WP J19. The momentary switch is used in the calibration of the High Power Leveler, discussed in Section V.C.

Refer to Figure A.3, Sheet 3, Appendix A. The voltage from the detector is compared with a reference voltage from TR1; this comparison is made via a resistor summing junction at the input to operational amplifier, U15. Any error voltage resulting from this comparison is integrated by U15 and C22. D1 is a 7.5 volt Zener diode, used to prevent U15 from swinging to too high a voltage. The output of the integrator is inverted in U14 so that correct polarity is achieved at the output of the leveling circuit.

To understand the function of U13, recall the discussion of how the unmodified AN/WSC-3 develops power control voltages. A potentiometer on the radio's front panel is adjusted and the resulting wiper voltage is sent

to AN/WSC-3 power circuits. The low voltage on the potentiometer is roughly 0.5 VDC. Within the AN/WSC-3, the voltage seen at the power control circuits is the difference between the wiper voltage and the low voltage on the potentiometer. U13 of the High Power Leveler is constructed as a differential amplifier. One input is the integrated and inverted error voltage from U14; the other input is connected to the AN/WSC-3 power control potentiometer via WP J19 and WP J17. The differential amplifier acts to negate any fluctuations (due, perhaps, to ground loops) seen at the low end of the power control potentiometer. This is an important feature since a very steady output power is desired of the AN/WSC-3, and small fluctuations in the leveling circuit may lead to significant variations of output power.

TR2 and D2, located between U13 and U14, provide a limit control on the maximum power level. When the High Power Leveler is calibrated, TR2 is adjusted to some threshold. If the voltage into U13 exceeds this threshold (by the diode's own threshold voltage) D2 conducts, thus limiting the voltage seen at the input to the differential amplifier.

The output of U13 is the power control voltage and is connected to WP J19. From there it is routed to the AN/WSC-3 via WP J17 and the frequency control modification discussed previously. D4 blocks any negative current

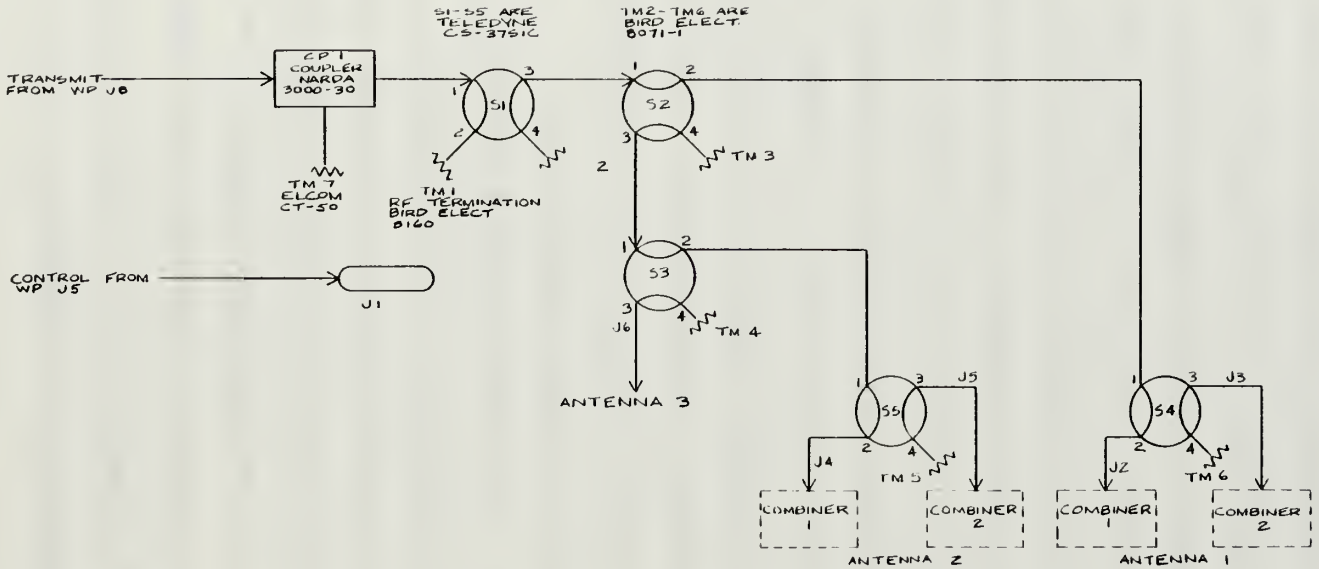
to the AN/WSC-3. R17 allows the discharge of a capacitor in AN/WSC-3 module A1A10 which, if not discharged, results in improper biasing of transistors inside the AN/WSC-3 power control circuits.

The speed of response of the High Power Leveler was measured by pulsing the 1 dB control line of the DAICO attenuator. The resulting RF power was sampled and converted to a voltage with an HP33330B detector. Detector output was then displayed on an oscilloscope. By measuring the rise and fall times of the detector wave form, the speed of the leveler is determined. The experiment was conducted over the entire range of power output and at pulse rates up to 100 Hz. The time from peak detector output to minimum detector output was measured as 2.5 mSec. under all conditions; thus, 2.5 mSec. is determined to be the speed of response of the leveling circuit. The response time of the DAICO programmable attenuator is specified as 5 mSec. and is therefore the limiting factor in the application of the High Power Leveler. That is, a time of 5 mSec. must elapse between giving a power command and making any measurements.

c. Antenna Selection

RF power from the output port of the directional coupler, CP2, used in the High Power Leveler is sent to the RF Switching Panel (RS). RS provides the transfer switches

which route transmitted power to one of the three antennas or into a dummy load mounted on RS. Figure A.12, Appendix A, is a schematic diagram of RS. Figure 5.4 is a block diagram. The directional coupler, CP1, shown in the figure is provided for calibration and testing purposes. A power meter may be connected to the COUPLE port if RF power measurement is desired. TM1 through TM66 are 100-watt coaxial terminations. TM1 is the dummy load into which transmitted power is dumped if DUMMY LOAD is selected instead of one of the antennas. TM2 through TM5 are located so as to provide terminations for the antennas to which the transfer switches are connected. Transfer switch S1 routes transmitted power either to a dummy load or to S2. Switch S2 routes power to S3 or S4. S4 selects between combiner 1 or combiner 2 of Antenna 1. If S3 is selected, it is used to route power directly to Antenna 3 or to switch S5. S5 selects between combiner 1 or combiner 2 of Antenna 2. The combiners feed separate halves of the QUAD OE-82 to prevent intermodulation products. Intermodulation products are severe when transmitting over certain channels simultaneously in the same OE-82. These channels are pre-determined according to the frequency plan in effect, and are assigned to different halves of the QUAD OE-82, eliminating the intermodulation products. Thus the need for two combiners.



REVISION LTR		DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY
A	DATE 8/1/80	NAVAL POSTGRADUATE SCHOOL
B	DATE 2/17/82	MONTEREY CALIFORNIA
	DATE	RF SWITCHING PANEL (RS) BLOCK DIAGRAM AND SCHEMATIC
	DATE	
	DATE	
DRAWN BY LS	DATE 2/1/80	DRAWING NUMBER RS-C-00 — SHEET 1 OF 2
APPROVED BY	DATE	

FIGURE 5.4

Antenna selection control arrives at RS J1 from WP J5; one control line exists for each of the five switches. The five control lines are generated on the Test Transmitter board. See Figure A.3, Sheet 3, Appendix A. CBL11 provides three bits of antenna control to the Test Transmitter board. Of these three (b_0, b_1, b_2), b_0 selects between combiner 1 or combiner 2 on both RS S4 and RS S5. b_0 is connected directly to pins 6 and 7 of U18 which in turn drives RS S4 and RS S5. Table 5.4 lists the decoding law for b_1 and b_2. In the table, a "0" in the columns under S1, S2 or S3 indicates the failsafe position of the transfer switch. A "1" in these columns indicates the energized (or switched) position. "1's" and "0's" in the b_1 or b_2 columns indicate standard, TTL positive true logic. The columns under S1, S2 and S3 indicate the position that these switches must be in to achieve the desired signal flow. From Table 5.4 the following control law is derived:

$$S_1 = b_1 + b_2$$

$$S_2 = b_2$$

$$S_3 = b_1 \cdot b_2$$

U16, 7408, and U17, 7432, on the Test Transmitter board are used to decode b_1 and b_2 according to this control law. The resulting outputs are sent to U18, ULN2003, which

TABLE 5.4

CONTROL BIT		DESIRED SELECTION	REQUIRED SWITCH POSITION		
b_2	b_1		S1	S2	S3
0	0	DUMMY LOAD	0	X	X
0	1	ANT. 1	1	0	X
1	0	ANT. 2	1	1	0
1	1	ANT. 3	1	1	1

TABLE 5.5

b_2	b_1	b_0	SELECTION
0	0	0	Dummy Load*
0	0	1	Dummy Load*
0	1	0	Antenna 1 Combiner 1
0	1	1	Antenna 1 Combiner 2
1	0	0	Antenna 2 Combiner 1
1	0	1	Antenna 2 Combiner 2
1	1	0	Antenna 3*
1	1	1	Antenna 3*

*Combiner selection has no meaning and hence is arbitrary.

drives the transfer switches. Table 5.5 summarizes the three antenna control bits and the resulting selection.

In addition to the five control lines, the cable between WP J5 and RS J1 carries five indicator lines. At RS, one each of these lines is attached to a relay contact in each transfer switch. The other contact of the relay is connected to ground. If the transfer switch is in the failsafe position the indicator line is allowed to float (and is in fact held at +5 VDC by a pull-up resistor). When the transfer switch is energized, the indicator lines are routed from RS J1 to WP J5 then to WP J2 and finally to Control Motherboard I via TUI J7. Figure A.7, Appendix A, illustrates this as well as all other TEST UNIT cable connections.

At CMB-I, these five lines are routed first to TUI J7 as status lines (status is discussed in Chapter VII) and then to logic circuits for indicator lamp control. Four such lamps are provided on the TEST UNIT panel to indicate to the operator that transmitted RF power is present at either the Dummy Load, Antenna 1, Antenna 2 or Antenna 3. Control for these indicator lamps comes from lamp dirver U16 on Test Board II. See Figure A.2, Sheet 4, Appendix A. The inputs to the pins of U16 are the result of the logical AND of the RF keyline and the lamp select lines from CMB-I. See Figure A.4, Appendix A, for a schematic diagram of CMB-I. U1, 7404, and U2, 7408,

convert the indicator lines from RS S1, RS S2 and RS S3 into lamp select lines according to the following decoding law (Positive Logic):

$$\text{Dummy Load} = S1$$

$$\text{Antenna 1} = \overline{S1} \cdot S2$$

$$\text{Antenna 2} = \overline{S1} \cdot \overline{S2} \cdot S3$$

$$\text{Antenna 3} = \overline{S1} \cdot \overline{S2} \cdot \overline{S3}$$

This law is derived by determining the state of the indicator lines when the transfer switches are set for a given destination.

d. RF Keyline

In order to key the AN/WSC-3 in the REMOTE mode a TTL LOW signal must be present at RT J2 pin 33. The RF keyline signal is generated on Test Board II and then sent to the Test Unit Interface panel (TUI). From TUI J7 it goes to WP J2, then to WP J12 and finally to RT J2.

Generation of the RF keyline parallels the generation of the Receiver Test signal ON-OFF control. See Figure A.3, Sheet 4, Appendix A. Three events must occur. First, the transmitter enable control bit of CBL12 goes high, removing the $\overline{\text{CLEAR}}$ line of U15, 7474. Second, the manual "XMTR ENABLE" pushbutton on the TEST UNIT panel is pressed, causing a clock pulse at U15, thus toggling the flip-flop to the HIGH logic state. Third, the output of the flip-flop is logically AND'ed in U14

with the transmitter on-off control bit. (See Appendix B for a list of the functions of each bit of CBL12.) The output of U14, a TTL HIGH for keyline on, is sent to CMB-I. Here it is logically NAND'ed in U6, 7400, with the complement of the CPU TIMEOUT signal. If CPU TIMEOUT is valid (TTL LOW) its complement is HIGH. Thus, two HIGH inputs to U6 on CMB-I results in the TTL LOW required at the keyline input to the AN/WSC-3. If either the CPU TIMEOUT signal or the output of the keyline control logic on Test Board II is in the off state, the AN/WSC-3 cannot be keyed. Generation of CPU TIMEOUT is discussed in Section IV.A.4.

e. Generation of External Modem

As previously discussed, the SSA uses the AN/WSC-3 to transmit a CW or PSK signal, and does so through use of an external modem. Although the AN/WSC-3 can provide the same transmit capabilities with its own internal modem, it can do so only on 25 kHz channel centers. The SSA requires the ability to transmit over any frequency in the up-link band. By employing an external modem and perturbing the 70 MHz carrier as discussed in paragraph a, above, the frequency restriction is removed. Table 5.1 lists specifications for the external modem; frequency is 70 MHz ± 250 kHz, power is 0 dBm ± 1 dB.

The 70 ($+\Delta_x$) MHz signal is generated in LO5, one of eight SSA local oscillators. LO5 is a Rockland frequency synthesizer and is programmed by the SSA's CPU via CBL5. The local oscillator signal enters the TEST UNIT at WP J7, which is the input to 10 dB directional coupler, CP1. The "OUTPUT" port of the coupler is connected to the AN/WSC-3 receive hardware on WP. The "COUPLE" port is connected to the external modem chain. See Figure 5.5 for a block diagram of WP. The 70 MHz signal out of the coupler is band-pass filtered in FL1 then applied to MOD1, a PSK modulator. Discussion of the data input to the PSK modulator follows. The output of the PSK modulator is amplified in AMPL3, band-pass filtered in FL3, then applied to RT J5, the external modem input to the AN/WSC-3. During receive operations, the signal at WP J7 is at 90 MHz. The coupled portion of this signal is sharply attenuated by the two 70 MHz band-pass filters, so the input to the external modem port is essentially zero.

Data to the PSK modulator originates at the Test Transmitter board. See Figure A.3, Sheet 2, Appendix A. Three modulating signals are available: a constant TTL HIGH for CW modulation, internally generated data from a maximum length sequence generator on the Test Transmitter board, and externally generated data from the HP1645A Data Error Analyzer. Selection of the data source and the design of the maximum length sequence generator is identical

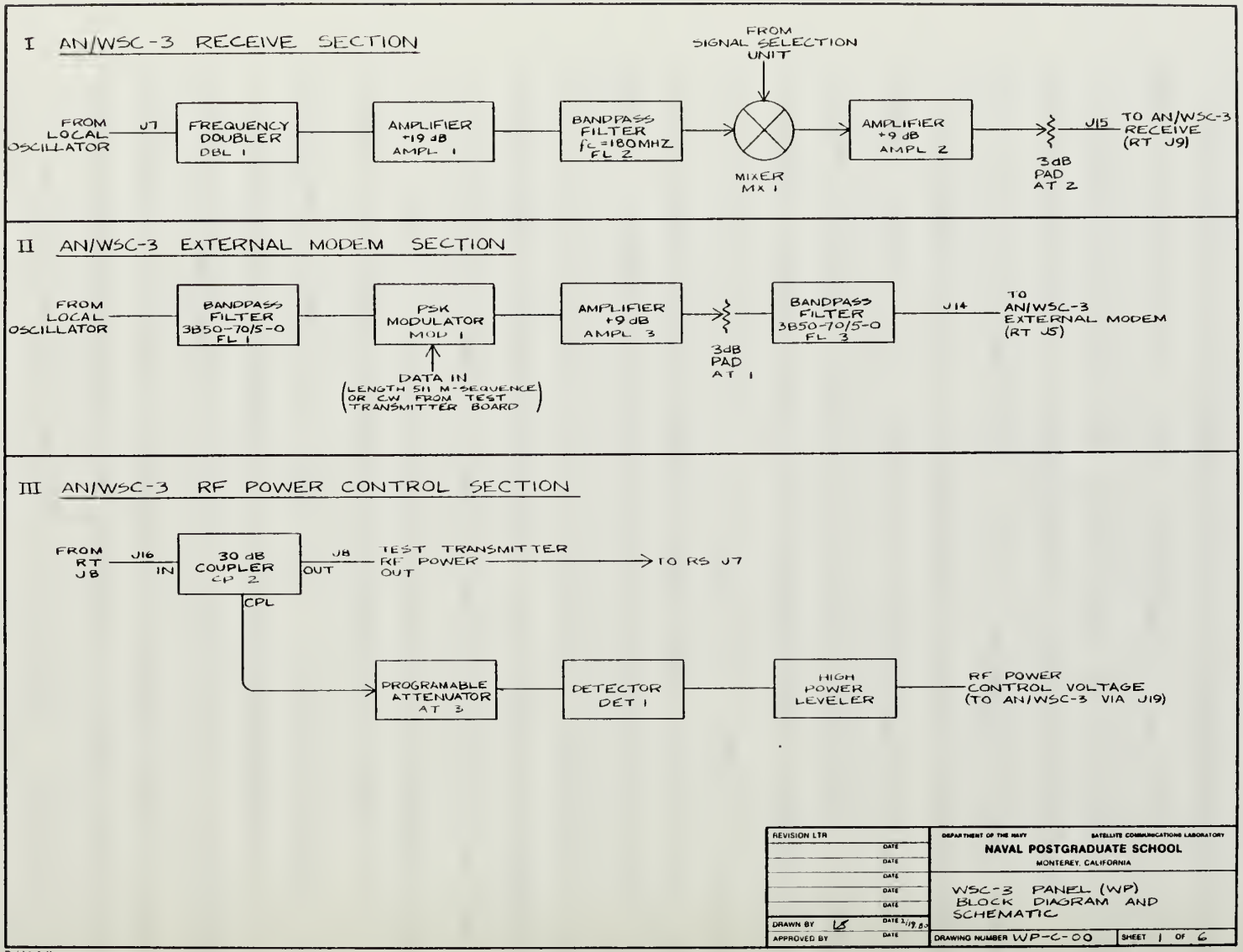

I AN/WSC-3 RECEIVE SECTION
FROM SIGNAL SELECTION UNIT
FROM LOCAL OSCILLATOR
J7
FREQUENCY DOUBLER DBL 1
AMPLIFIER +19 dB AMPL 1
BANDPASS FILTER fc=180MHZ FL 2
MIXER MX 1
AMPLIFIER +9 dB AMPL 2
3dB PAD AT 2
J15
TO AN/WSC-3 RECEIVE (RT J9)
II AN/WSC-3 EXTERNAL MODEM SECTION
FROM LOCAL OSCILLATOR
BANDPASS FILTER 3B50-70/5-0 FL 1
PSK MODULATOR MOD 1
DATA IN (LENGTH 511 M-SEQUENCE OR CW FROM TEST TRANSMITTER BOARD)
AMPLIFIER +9 dB AMPL 3
3dB PAD AT 1
BANDPASS FILTER 3B50-70/5-0 FL 3
J14
TO AN/WSC-3 EXTERNAL MODEM (RT J5)
III AN/WSC-3 RF POWER CONTROL SECTION
FROM RT J8
J16
IN
30 dB COUPLER CP 2
OUT
J8
TEST TRANSMITTER RF POWER OUT
TO RS J7
CPL
PROGRAMABLE ATTENUATOR AT 3
DETECTOR DET 1
HIGH POWER LEVELER
RF POWER CONTROL VOLTAGE (TO AN/WSC-3 VIA J19)
REVISION LTR
DRAWN BY
APPROVED BY
DEPARTMENT OF THE NAVY
SATELLITE COMMUNICATIONS LABORATORY
NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA
WSC-3 PANEL (WP) BLOCK DIAGRAM AND SCHEMATIC
DRAWING NUMBER WP-C-00
SHEET 1 OF 6

FIGURE 5.5

to that discussed in Section V.A.1, for the Receiver Test Section. The exception is that control for the external modem data comes from CBL11 vice CBL12, and the circuitry is contained on the Test Transmitter board vice Test Board I.

The selected data is routed from the Test Transmitter board to the PSK modulator via WP J19. The data is also buffered in U20 of the Test Transmitter board (Figure A.3, Sheet 2, Appendix A) and brought out via WP J19 to a monitor on the Data Interface. Details of the Data Interface are discussed in Chapter VI.

B. APPLICATION AND TESTING

1. AN/WSC-3 Setup

Before the AN/WSC-3 may be used under SSA control, the following settings must be made on the transceiver's front panel:

PRIMARY POWER	ON
OPERATE/STANDBY	OPERATE
SATCOM/LOS	LOS
REMOTE/LOCAL	REMOTE
FREQUENCY SELECT	PRESET
TEST KEY	OFF

Additionally, within the AN/WSC-3, two toggle switches must be positioned. Both are immediately behind the front panel and are accessed by loosening the panel mounting bolts and sliding the radio partially out of its cabinet.

The Frequency Standard switch should be placed in the "EXTERNAL" position and the AN/WSC-3 modification switch should be placed in the "WSC-3 MODIFIED" position.

2. Control

The AN/WSC-3 is controlled from the SSA TOUCH PANEL. The operator uses the Touch Panel to access menus for AN/WSC-3 receive, transmit and power balance functions. Each of these menus prompts the operator in step-by-step fashion as to desired channel or frequency, modulation format, PSK data rates, antenna to be used and power level if transmitting.

During AN/WSC-3 receive operations, the operator first selects the antenna to be monitored. This selection further fixes the satellite to be monitored as each antenna is normally pointed at a different satellite. The operator next selects the channel or frequency that is to be monitored and finally the demodulation mode to be used. Received signals may be observed at the DATE INTERFACE, LOUSPEAKER, TAPE RECORDER or TEST UNIT scope as chosen by the operator.

During general up-link operations, the operator uses the TOUCH PANEL to make selections similar to those listed above for receive; additionally, desired power level is selected. The operator is then prompted as to how to key the transmitter on and off. Detailed instructions and a copy of the displays observed by the operator on the TOUCH PANEL during transmit and receive operations are contained in Appendix G.

If desired the operator may operate the AN/WSC-3 in the local mode, vice remote. To do so, the REMOTE-LOCAL switch on the radio is placed in the LOCAL position. This action returns control of moudlation mode and transmitted power level to the respective knobs on the AN/WSC-3. Frequency may be established in only the MANUAL mode. Antenna selection is still made via the SSA TOUCH PANEL. If the AN/WSC-3 is to be used in the local mode for reception, the local oscillator signal, LO5, at WP J7 must be set to 90 MHz.

3. Power Balance

One of the primary applications of the AN/WSC-3 within the SSA is the conduct of power balancing. In a power balance, a reference or measuring station attempts to determine the effective isotropic radiated power (EIRP) of some remote ship or station through spectrum analysis techniques. To understand how this is accomplished, two characteristics of hard-limiting transponders are considered. (The transponders in current NAVY SATCOM satellites are hard-limiting.) First, if two downlink signals occupying the same hard-limiting transponder appear at the same level on a spectrum analyzer, the two signals are of the same EIRP. Second, if one of the signals increases in amplitude, the other will decrease a corresponding amount (and vice versa). If a reference station wishes to measure the EIRP of some remote station, the reference station instructs the remote station to transmit a CW signal in a particular channel. The reference station transmits a CW signal in the same transponder and adjusts its

own power until the observed downlink powers of the signals are identical. The reference station then determines its own EIRP and hence, that of the remote ship or station.

The SSA uses the AN/WSC-3 to generate a reference signal for power balancing and uses one of the SPECTRUM RECEIVERS and the array processor to automatically determine a remote station's EIRP. The SSA's CPU adjusts reference power, calculates EIRP and displays the result to the operator. During the conduct of the power balance, the operator is prompted as to antenna and channel selection and as to starting and halting transmission of the reference signal. Detailed instructions to the operator, a flow-chart of the power balance operation and copies of the displays observed on the TOUCH PANEL are contained in Appendix G.

C. MEASUREMENT AND CALIBRATION

1. High Power Leveler Adjustment

The High Power Leveler requires two adjustments; one is for maximum power output, the other is adjustment of the nominal reference voltage at the input to the leveler. Both adjustments require that the AN/WSC-3 be transmitting RF power. Instructions for setting up a transmitted signal are discussed in Section V.B, and Appendix G. These instructions should be followed to apply a +20 dbW signal into the DUMMY LOAD; once this is accomplished, adjustments may be performed.

If the High Power Leveler were to fail, a situation may arise where the power control voltage to the AN/WSC-3 rises to too high a level, thus allowing RF power to exceed a safe limit and resulting in damage to internal circuits. The situation is avoided by limiting the voltage that can appear at the input to differential amplifier, U13 on the Test Transmitter Board. See Figure A.3, Sheet 3, Appendix A. Potentiometer TR 2 is used to set this voltage. The adjustment is made by depressing the momentary switch mounted on WP J19. TR2 is adjusted while observing the RF power meter on the front panel of the AN/WSC-3 or a power meter attached to RS J8. The potentiometer is turned until the AN/WSC-3 power meter reads 22 dbW or the meter at RS J8 reads 22 dBm.

To adjust the nominal reference voltage at the input to the High Power Leveler, a 20 dbW transmit level is set up according to the instructions contained in Section V.B.2 and Appendix G. A power meter is attached to RS J8, and is observed while potentiometer TR1 is adjusted. TR1 is turned until the power at RS J8 is 20.4 dBm; this level at RS J8 indicates a level of 20 dbW at the output of the directional coupler on RS.

At this point, the system is calibrated to provide 20 dbW at the input to the transfer switches on RS. During general up-link or power balance operations, it is the EIRP at the transmit antenna that is of interest. EIRP is given by the sum of the power out of the AN/WSC-3, the cable/coupling

loss to the antenna and the antenna gain. Further, recall that each dB of attenuation commanded into the High Power Leveler results in a one dB increase in transmitted power. There are, however, slight variations between power command and actual transmitted power. The difference between the power command from the CPU via CBL-11 and the resulting EIRP is a calibration factor that is determined prior to operation and stored in memory. Then during AN/WSC-3 operation, the CPU calculates the power required to achieve the desired EIRP by subracting the calibration factor from the desired EIRP and applying the resulting power command via CBL-11.

Table 5.6 lists the actual power at RS J8 as a function of the power commanded by the CPU. From this table it is seen that output power is within 0.2 dB of commanded power. Cable loss and antenna gain must be determined for each antenna at each installation. A calibration factor for power balancing is easily determined by having a known reference perform a power balance against the SSA, for some known AN/WSC-3 power command. The reference station informs the operator of the SSA's EIRP and the calibration factor is the difference between EIRP and the known power command.

2. Transponder Power Calibration

A final calibration factor is needed to determine the EIRP at a satellite transponder. The power seen at an earth sation's antenna is given by

$$C = EIRP_{sat} + L_{FS} + G_R \qquad (5.1)$$

TABLE 5.6

POWER COMMAND	POWER AT RS J8 (dBW)	AN/WSC-3 POWER METER INDICATION (dBW)
0	0.1	OFF SCALE
1	1.1	OFF SCALE
2	2.1	0
3	3.0	2
4	4.0	3
5	5.0	4
6	6.0	5
7	7.0	7
8	8.2	8
9	9.1	10
10	10.1	11
11	11.1	12
12	12.0	13
13	13.0	14
14	14.0	15
15	15.0	16
16	16.1	17
17	17.1	18
18	18.1	19
19	19.0	20
20	20.0	21

If C is measured and L_{FS} and G_R are known, it is easy to solve for EIRP. G_R is the receiver antenna gain and is known at the earth station. L_{FS} is free-space loss and is given by

$$L_{FS} = (\lambda/4\pi R)^2 \qquad (R.2)$$

R is range, in meters from the receive antenna to the satellite; λ is the signal wavelength in meters. A calibration factor is calculated from L_{FS} and G_R and entered into CPU memory at time of installation.

VI. DATA INTERFACE SECTION

This section of the TEST UNIT consists of the HP1645A Data Error Analyzer, the Data Interface (CI) and the RS232 to TTL interface on Control Motherboard II. The Data Interface Section provides TTL level monitoring of Receiver Test signal data, external modem data, AN/WSC-3 received PSK data and received bit timing and it provides bit error rate testing of AN/WSC-3 received data or local TTL data. Additionally, the HP1645A provides data for use in Receiver Test signals and the external modem.

A. GENERAL DESCRIPTION

The Receiver Test and Test Transmitter data monitors were introduced in Sections IV and V respectively. In both cases the input lines to the PSK modulators are passed also to a 7404 inverter whose outputs are the data monitors. The outputs of these inverters are routed to the WSC-3 panel (WP) where they are sent to WP J11. From WP J11 they go to DI J1, then the BNC feedthru connectors where the signals are accessed for monitoring.

Figure 6.1 is a block diagram of the Data Interface section. Received PSK data in the AN/WSC-3 is recovered at RT J2, pin 67 and is routed to WP J12. From WP J12 the recovered data goes to Control Motherboard II (CMB-II) where it is converted from RS 232 to TTL levels. The TTL data then is sent to DI J1 via WP J11 and is fed to the appropriate BNC feedthru connector.

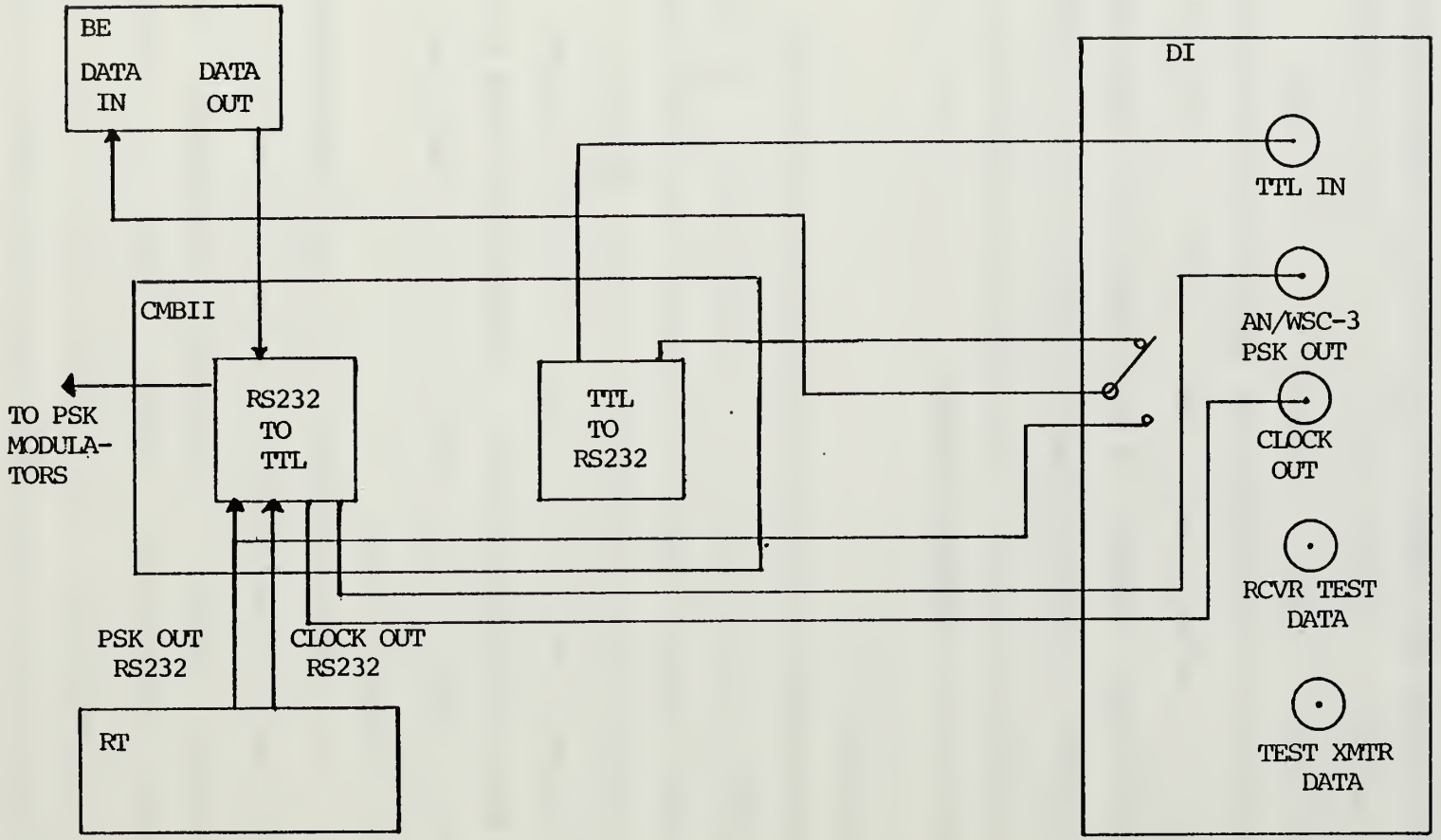

BE
DATA IN
DATA OUT
DI
TTL IN
CMBII
AN/WSC-3 PSK OUT
TO PSK MODULA-TORS
RS232 TO TTL
TTL TO RS232
CLOCK OUT
RCVR TEST DATA
PSK OUT RS232
CLOCK OUT RS232
RT
TEST XMTR DATA

FIGURE 6.1

Received bit timing is recovered at RT J2, pin 76 and follows a similar path. The RS 232 level data from the AN/WSC-3 is also applied to one terminal of SPDT switch at DI. The purpose of this switch is explained later.

Data from the HP1645A is an RS 232 level maximum length sequence of length and clock rate set on the front panel of the HP1645A. This data is sent to the RS232 to TTL interface on CMB-II. From here it is routed to the data selection logic for the Receiver Test section and the external modem.

The EXTERNAL TTL input at DI is routed to CMB-II where it is converted to RS 232 levels; the resulting signal is returned to DI and connected to the second terminal of the SPDT switch previously mentioned. The common terminal of this switch selects either AN/WSC-3 received data or externally input data and routes the selected signal to the HP1645A via CMB-II.

Operator interface with the HP1645A is intended to be limited to signal input at the Data Interface and selection of clock rate and sequence length on the HP1645A. All electrical and signal inputs to the HP1645A are affected at the RS 232 interface connector at the rear of the device. All inputs and outputs at the Data Interface are TTL; all TTL/RS 232 conversion is made on CMB-II.

B. CIRCUIT ANALYSIS

Figure A.4, Appendix A is a schematic diagram of CMB-II. The TTL to RS 232 interface shown in Figure 6.1 consists of U3, 8T15 on CMB-II. The input to U3 is the EXTERNAL TTL input from DI; it arrives at U3 via WP J11 pin 15. The output is routed back to DI via WP J11 pin 13. At DI, this RS 232 level signal is connected to one terminal of DI s1. See Figure A.13, Appendix A, for a schematic diagram of DI.

The RS 232 to TTL interface shown in Figure 6.1 consists of U1 and U2, 8T16's, of CMB-II. U1 converts RS 232 data from the HP1645A to TTL level data for the Receiver Test section and the AN/WSC-3 section. Recall that this data is one of three possible inputs to the PSK modulators utilized in those sections. U2 converts received PSK data and receive bit timing signals from the AN/WSC-3 from RS 232 to TTL for output at the Data Interface.

C. APPLICATION AND TESTING

To use the Data Interface to monitor signals, the operator need only connect an oscilloscope or other test device to the BNC feedthru connectors on DI. An oscilloscope is always available on the TEST UNIT panel; one channel of the Tektronix 7A18 is connected to the AUDIO SELECTOR, but the second channel of this dual-trace

amplifier is available for use. To utilize this feature, the operator must select VERT MODE and TRIG SOURCE "LEFT" on the Tektronix 7613 mainframe and select CH 2 on the 7A18. A coaxial cable with BNC connectors is then used to connect the desired data monitor to the input of the oscilloscope. To use the HP1645A for bit error rate testing, the operator selects the source to be monitored via the switch on DI: the AN/WSC-3 or an external TTL data source. An external source is applied at the appropriate BNC connector; the AN/WSC-3 is internally connected. The clock rate and sequence length of the HP1645A is then set to match that of the incoming data. Resulting bit error rates are shown on the HP1645A display. Detailed instructions on the use of the HP1645A are contained in the operation and maintenance manual for that device.

The Data Interface section is tested by using an oscilloscope to detect the presence of the Receiver Test and Test Transmitter data and the presence of AN/WSC-3 PSK data with a known PSK signal applied to the AN/WSC-3. The HP1645A can quickly be tested by sliding the OFF-LOOP switch to the LOOP position; this results in the HP1645A recovering and testing its own data sequence. No errors should be displayed. Instructions for troubleshooting the Data Interface section are found in Appendix C.

VII. STATUS SIGNALS

The TEST UNIT provides twelve status lines at GI-J5 (Gate Interface) where they are then routed to a DR 11C via the Control Interface. The purpose of this chapter is to discuss the generation of the TEST UNIT status signals.

A. DESCRIPTION

Table 7.2 lists the twelve TEST UNIT status signals. These signals are generated at various points throughout the TEST UNIT; they are consolidated at Control Motherboard I (CMB-I) and routed to GI J5 via TUI J9. Each status line is negative true TTL.

B. GENERATION OF STATUS SIGNALS

1. AN/WSC-3 Status

As discussed in Section V, the RF keyline is generated on Test Board II. See Figure A.2, Sheet 4, Appendix A. Pin 6 of U14, 7408 is used as the RF keyline. Note that this line is also applied to U17, 7404; the output of the inverter (used as a buffer) is the negative true keyline status. The other three status lines originate within the AN/WSC-3 and are brought out via RT J2 and J3. From these jacks the lines are routed to CMB-I via WP. RT J2, pin 38 is normally open, but is grounded if RF output power exceeds 1 Watt. This RF power

TABLE 7.2

TEST UNIT STATUS

AN/WSC-3 IN REMOTE MODE

AN/WSC-3 IN OPERATE MODE

AN/WSC-3 KEYLINE ON

AN/WSC-3 POWER > 1 WATT

RS S5 ENERGIZED

RS S4 ENERGIZED

RS S3 ENERGIZED

RS S2 ENERGIZED

RS S1 ENERGIZED

RECEIVER TEST ENABLED

HIGH POWER LEVELER FAULT

LOW POWER LEVELER FAULT

All signals are active low TTL.

indication enters CMB-I (Figure A.4, Sheet 1, Appendix A) at TUI J7, pin 23. Here it is held at +5 VDC by a pull-up resistor, R13, until pin 38 of RT J2 is grounded. The remote mode and operate mode originate at RT J3, pin i and RT J2 pin 38 respectively. Pin 38 is "open" in standby, and +28 VDC in operate. Likewise, pin i is open in LOCAL, and +28 VDC in REMOTE. As seen on the schematic for CMB-I, each of these lines is used to drive a transistor switch. If the line to the base of the transistor (Q1 and Q2) is open, no current flows into the base and the transistor is "off". Thus the collector, and hence the status line, is at +5 VDC. If the input to the series resistor at the base is at +28 VDC, the current through the base is sufficient to drive the transistor into the saturation region; the transistor conducts and the collector, as well as the status line, is at ground.

2. Transfer Switch Status

The five transfer switches on the RF Switching Panel (RS) each have a relay whose contact position depends on whether the transfer switch is in the failsafe position or the energized position. The relay contacts are labeled A, B, and C. In the failsafe position, B is connected to C and A is open; in the energized position, A is connected to C and B is open. To develop an active low status signal, terminal C of each transfer switch is

tied to ground. Terminal A is routed to CMB-I via WP and is held at +5 VDC by a pull-up resistor on CMB-I (R8-R12). Terminal A is then connected to the appropriate pin at TU J9. When the transfer switch is energized, A is connected to C and the status line is at ground.

3. Receiver Test Status

As discussed in Section IV, the Receiver Test control line is generated on Test Board II. See Figure A.2, Sheet 4, Appendix A. The Receiver Test on-off control is generated in U14, 7408. This positive-true control line is inverted in U17, 7404, to produce the Receiver Test status line. The output of U17 is routed to CMB-I, where it is then sent to TUI J9.

4. High and Low Power Leveler Fault

Circuitry for the generation of these status lines remains to be designed. Failure of a leveler might be indicated by the inability of the particular leveler to reduce an error voltage to zero. The speed of response of both levelers has been measured as discussed in Sections IV and V. Failure of a leveler might be detected by sensing the existence of error voltage over some period of time longer than the response time. If an error voltage exceeds some threshold over some period of time, the status line is activated. Another means of failure detection might come from sensing the existence of the leveler output voltage above some maximum threshold.

An ever-present error voltage results in a continuously rising integrator output. A third method would involve a comparison of output power. The nominal or commanded power is known; the actual power can be measured with a diode detector. By comparing detector output with desired output (after the leveler response time) a determination may be made as to whether the leveler is indeed functioning properly.

VIII. HARDWARE SUMMARY AND INTERACTION

The purpose of this chapter is to discuss the major hardware modules of the TEST UNIT and how they interact to support the five TEST UNIT sections previously discussed. Figure A.7, Appendix A shows the main TEST UNIT components and their cable connections. Parts lists, cable lists and wiring/pinout lists are contained in the Appendices.

A. TEST UNIT PANEL

The operator's interface with the TEST UNIT occurs at the SSA TOUCH PANEL and at the TEST UNIT Panel (TU). Figure 2.1 is a copy of the layout of this panel. Figure 8.1 is a block diagram of TU. The panel shown in Figure 2.1 covers a "drawer", mounted on rack slides, that houses the components shown in Figure 8.1.

Occupying the left half of TU is the Tektronix 7613, 7A18 and 7L12 oscilloscope and spectrum analyzer units. To the left is the receiver output thumbwheel; recall that this thumbwheel generates a three-bit BCD code that is routed to the AUDIO SELECTOR. The BCD code chooses one of five SSA receivers for display on the oscilloscope. Three leads from the thumbwheel are routed to TUI via TU J8. See Figure A.9, Sheet 3, Appendix A.

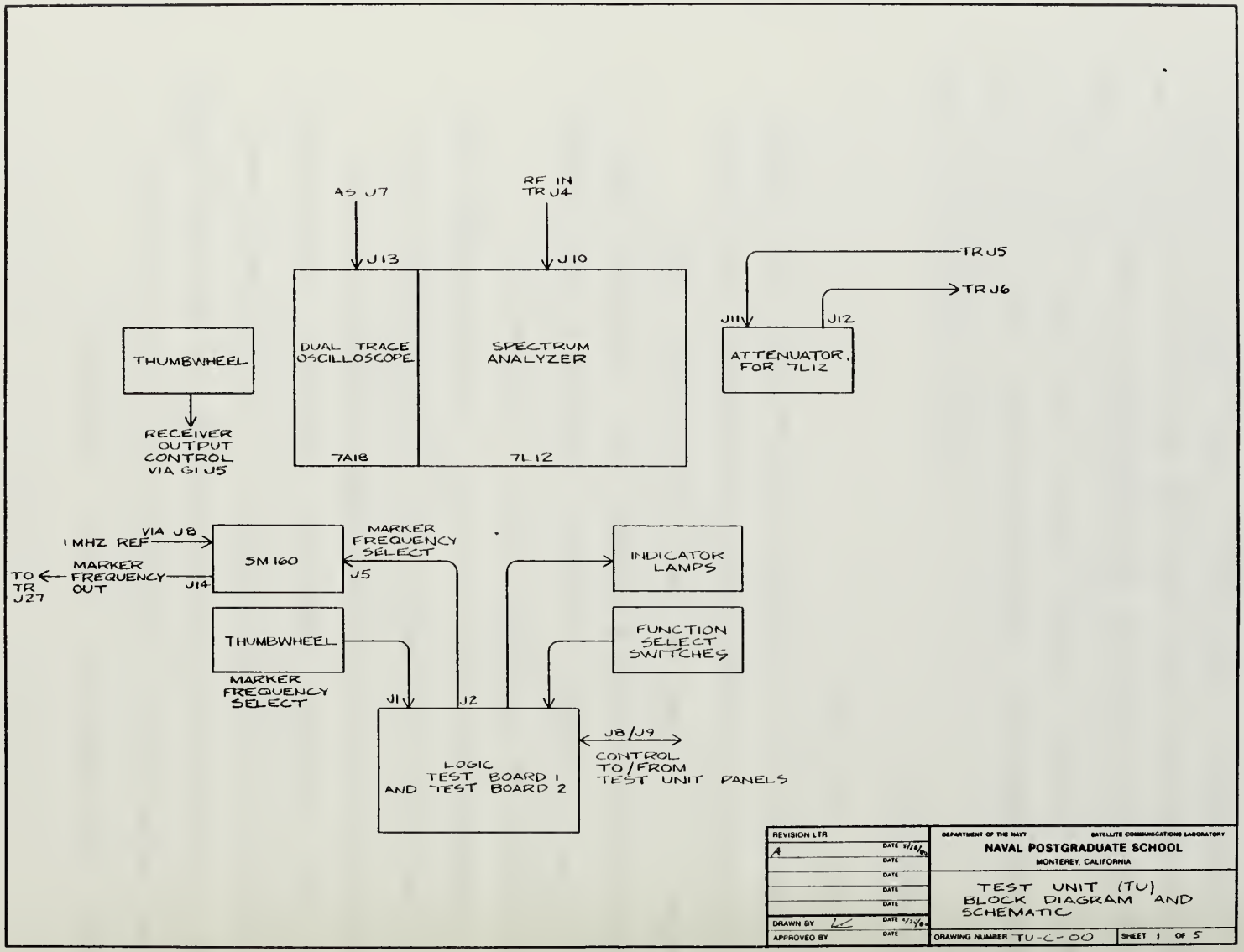

A5 J7
RF IN TR J4
J13
J10
TR J5
TR J6
J11
J12
THUMBWHEEL
DUAL TRACE OSCILLOSCOPE
SPECTRUM ANALYZER
ATTENUATOR FOR 7L12
7A18
7L12
RECEIVER OUTPUT CONTROL VIA G1 J5
VIA J8
1 MHZ REF
MARKER FREQUENCY SELECT
SM 160
INDICATOR LAMPS
TO TR J27
MARKER FREQUENCY OUT
J14
J5
THUMBWHEEL
FUNCTION SELECT SWITCHES
MARKER FREQUENCY SELECT
J1
J2
J8/J9
LOGIC TEST BOARD 1 AND TEST BOARD 2
CONTROL TO/FROM TEST UNIT PANELS
REVISION LTR
A
DRAWN BY
APPROVED BY
DEPARTMENT OF THE NAVY
SATELLITE COMMUNICATIONS LABORATORY
NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA
TEST UNIT (TU) BLOCK DIAGRAM AND SCHEMATIC
DRAWING NUMBER TU-C-00
SHEET 1 OF 5

FIGURE 8.1

To the top right of TU are three rows of pushbuttons, labeled Received RF, Transmitted RF and SSA IF. These pushbuttons select the signal that is to be displayed on the Tektronix spectrum analyzer. Below these switches the marker frequency thumbwheels, frequency invalid indicator and marker on-off switch are located. The thumbwheels provide BCD frequency control to the Syntest SM-160 frequency synthesizer which is mounted in a PC board cage immediately behind TU.

Beneath the marker frequency portion of TU are the Test Transmitter and Receiver Test enable pushbuttons. Also there are indicator lamps that display which antenna is being used for transmission or test signal input.

In the lower right section of TU is found the attenuation knob for the spectrum analyzer. This knob controls a 60 dB step attenuator which should be used whenever the overload indicator is on. The operator does not normally use the attenuation control that is found on the Tektronix 7L12; this knob should be turned to zero attenuation.

Finally in the bottom right corner is the Lamp Test switch; pushing this button energizes all lamps on TU so that faulty ones may be identified. All lamps on TU (with the exception of the two LED's) are industry standard 327 or 387 28 volt lamps used with 24 volts for very long life. One terminal of each lamp is connected to a common 24 VDC line; the other terminals are the control lines

and are connected to ULN 2003 lamp drivers on Test Board I and Test Board II. TTL level controls are generated by the various circuits on these boards; these control lines are the inputs to the corresponding lamp driver. A high level at the driver input activates the driver which then lights the lamp. In order to capture the operator's attention, selected lamps are blinked on and off at one second intervals. (These lamps include: Test Transmitter Enable, Receiver Test Enable, Marker ON and Frequency Invalid.) U16 on Test Board I (Figure A.1, Sheet 3, Appendix A) is a 555 timer, configured as an astable multivibrator. Its one Hertz output is logically AND'ed with the TTL control lines for the lamps mentioned above. Figure A.8, Appendix A, is a schematic of TU and shows the wiring of all lamps and pushbutton switches. Appendix E is a wire list and is useful in determining the source/destination of all connections on TU.

B. TEST UNIT RF PANEL (TR)

Figure A.9, Appendix A contains schematic diagrams of TR. This panel is used to mount the RF hardware (amplifiers, electronic switches, filters, etc.) used in the routing or generation of signals for the Spectrum Analyzer Section and the Receiver Test Section of the TEST UNIT.

C. AN/WSC-3 PANEL (WP)

This panel contains the RF hardware for AN/WSC-3 receive functions and generation of the external modem signal. Its schematic diagram is shown in Figure A.10, Appendix A. Mounted to this panel are the Test Transmitter board and Control Motherboard II (CMB-II). The Test Transmitter board provides data to the external modem for PSK modulation, an interface for CBL11 with the TEST UNIT, and the High Power Leveler used for automatic control of AN/WSC-3 transmit power. Control Motherboard II provides the TTL/RS-232 interface and acts as an interchange between several TEST UNIT modules. Specifically, the Data Interface panel, the HP1645A, the Test Unit Interface and WP all meet (via microribbon cable) at CMB-II.

D. RF SWITCHING PANEL (RS)

This panel houses the RF transfer switches used in routing transmitted power from the AN/WSC-3 to the desired antenna. It also provides a dummy load for the AN/WSC-3 and terminations for cables to antennas not in use.

E. DATA INTERFACE (DI)

This panel houses five BNC connectors that provide TTL-level monitoring of Test Transmitter and Receiver Test data, received PSK data and clock from the AN/WSC-3

and an external TTL input to the HP1645A Data Error Analyzer. Also provided is a toggle switch, used to select the input source for the HP1645A. This source may be the demodulated AN/WSC-3 PSK data or external TTL data. The HP1645A is used to perform bit error rate analysis, or to provide a source of data for Receiver Test signals or PSK transmission by the AN/WSC-3. Clock rate and sequence length are controlled manually from the front of the HP1645A.

F. AN/WSC-3 (RT)

The satellite communications transceiver is used to provide AM, FM, PSK or FSK demodulation, general up-linking and power balancing. RT may be operated under complete SSA control, partial SSA control by placing the radio in LOCAL, or it may be completely freed of SSA control and operated manually. The AN/WSC-3 interfaces primarily with WP.

G. TEST UNIT INTERFACE (TUI)

TUI consists of Control Motherboard I (CMB-I) and the panel to which it is mounted. CMB-I provides circuitry for the CPU TIMEOUT signal and relays for control of the Noise Temperature test. It provides an interface for CBL12 with the TEST UNIT. Like CMB-II, it is also an intersection point for several TEST UNIT assemblies: TU, TR and WP. Finally, CMB-I provides a consolidation

point for the twelve TEST UNIT status lines and routes them to the GATE INTERFACE via TUI J9.

H. TEST UNIT EXTERNAL INTERFACE (TXI)

. TXI is shown in Figure 4.7 and is used as an alternate means of providing Receiver Test signals. Mounted on TXI are three combiners, one for each antenna. One input to each combiner comes from the Low Power Leveler on TR. The other input comes via a 20 dB attenuator from a BNC connector also mounted on TXI, where the output of any desired signal source may be applied. The output of each combiner is routed to the corresponding antenna via the SSA Station Interface. The cable and coupling loss from the BNC connector to the input of the RF preamplifier at the antenna is labeled on TXI at the input connector.

IX. CONCLUSIONS

The TEST UNIT has been designed, constructed and integrated into the SATCOM Signal Analyzer. Further, it has been calibrated for use in the NPS installation of the SSA. The TEST UNIT is capable of the following:

a. Monitoring SSA signals in the time and frequency domain.

b. Generating self-test and calibration signals of precise frequency and amplitude.

c. Measuring system operating temperature.

d. Power balancing, general up-linking and signal reception with the AN/WSC-3 transceiver.

e. Bit error rate testing and data monitoring.

Remaining to be designed are the status signals indicating a failure of the LOW and HIGH Power Levelers. Discussion of these status signals is provided in Chapter VII as well as a few possible approaches to their design.

APPENDIX A

SCHEMATIC AND BLOCK DIAGRAMS

Figures A.1 through A.3 are schematic and block diagrams of the TEST UNIT modules already discussed.

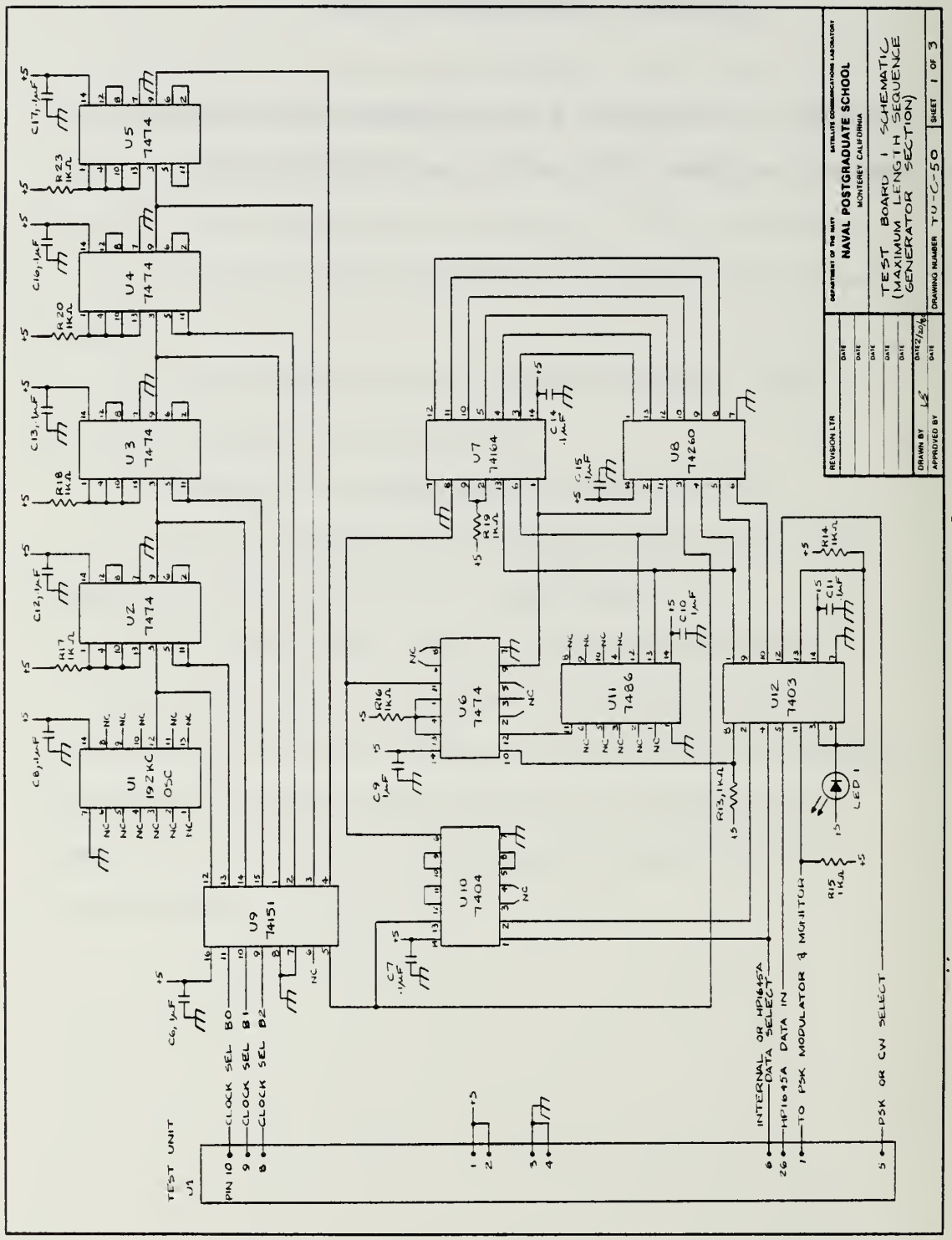


FIGURE A.1, SHEET 1

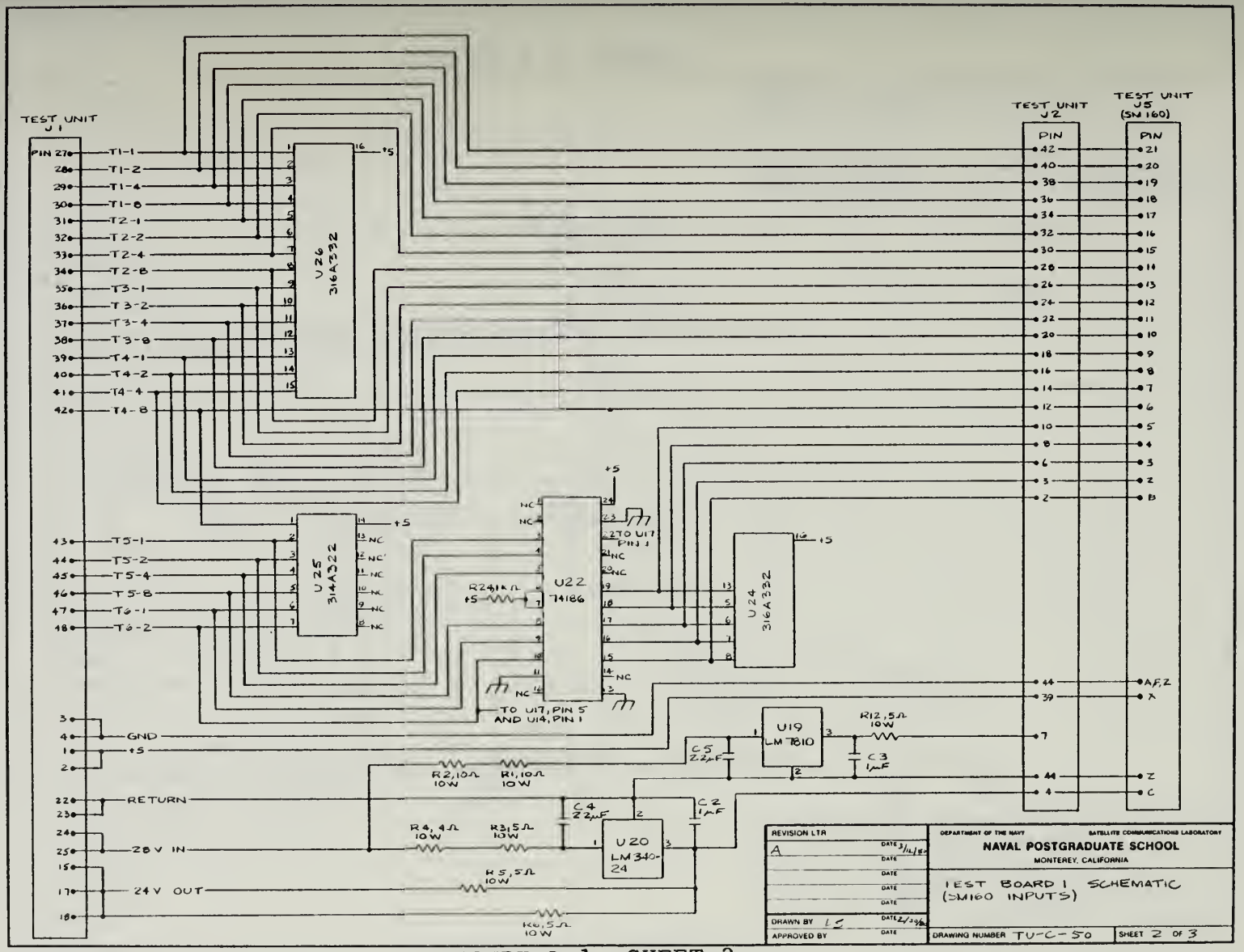


FIGURE A.1, SHEET 2

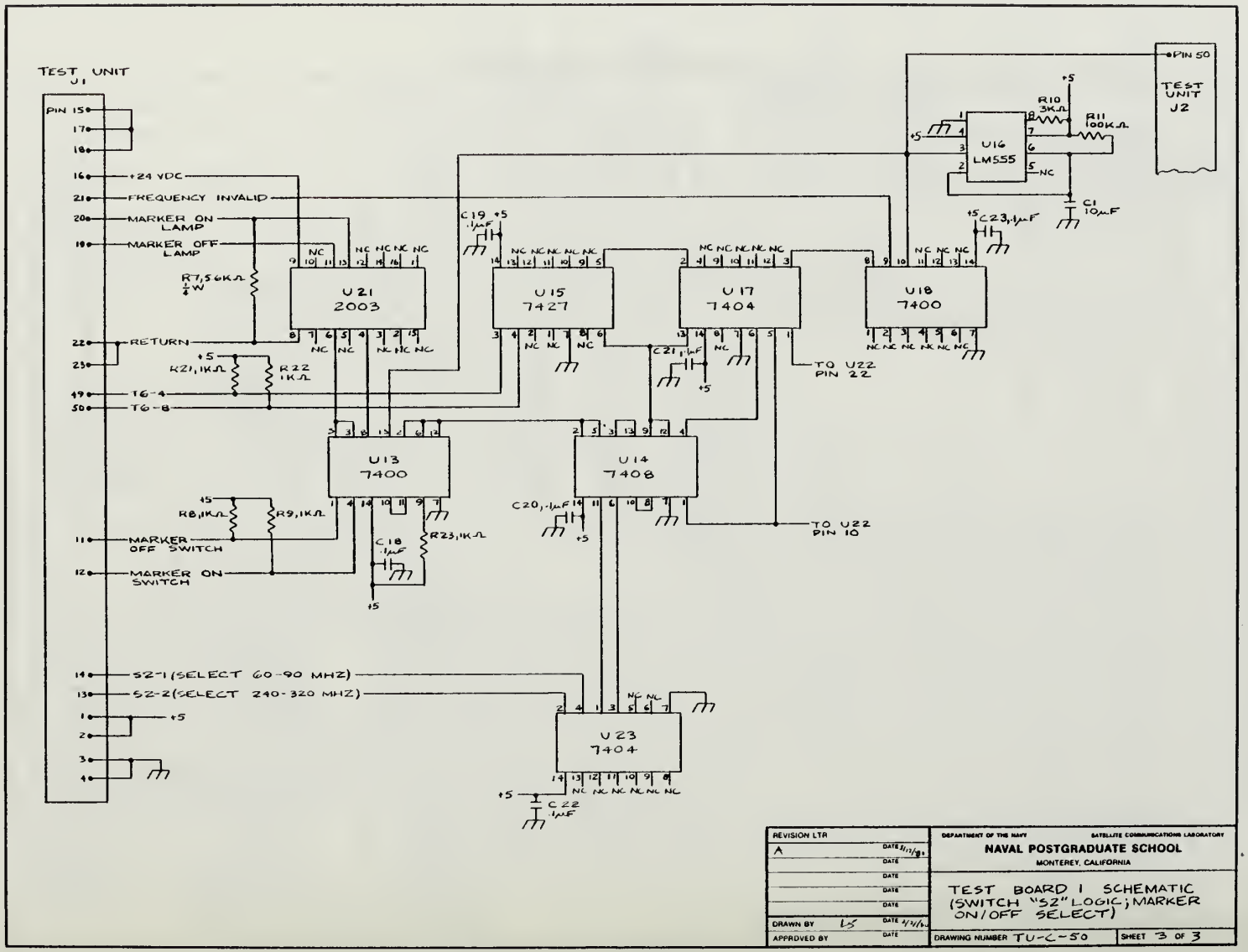


FIGURE A.1, SHEET 3

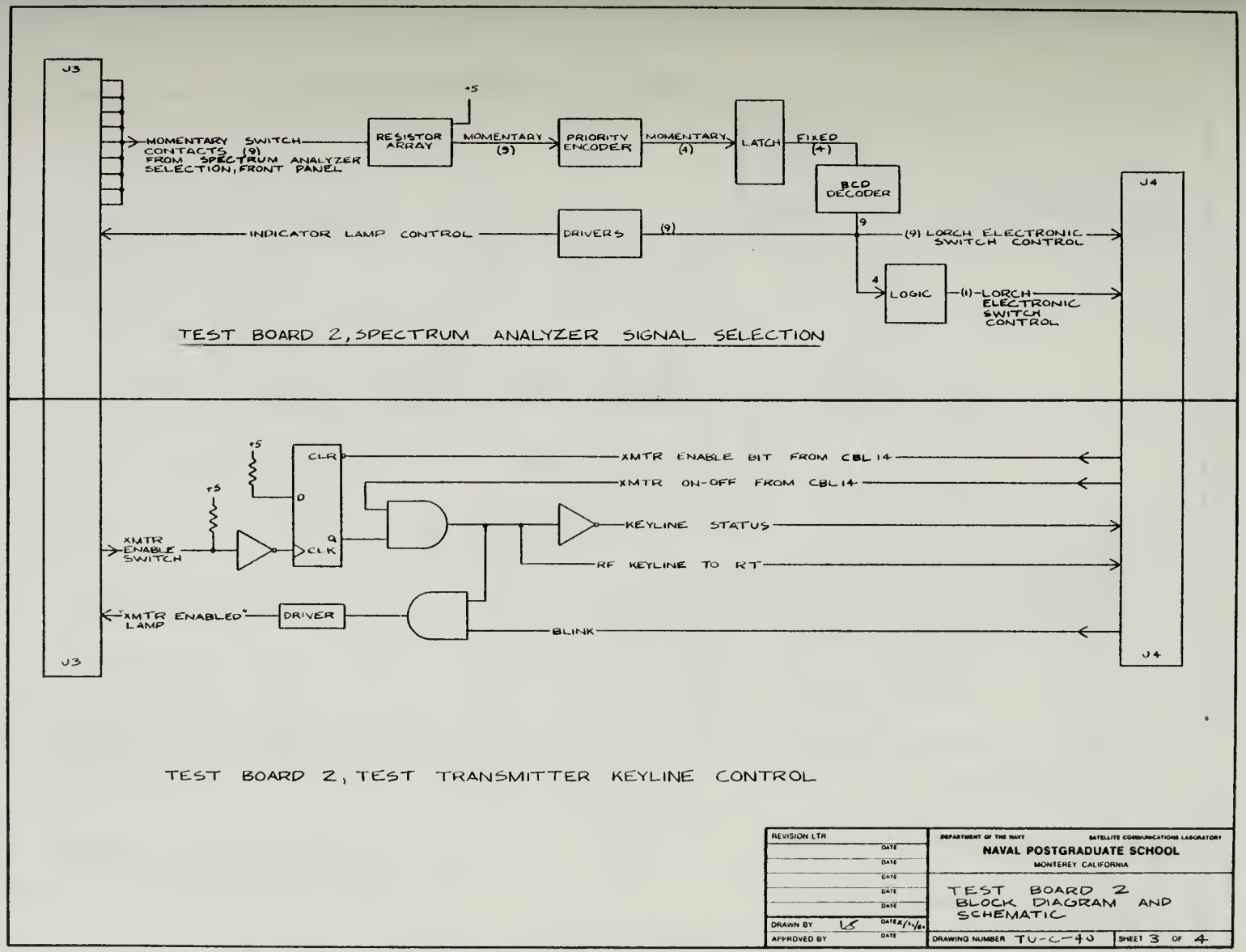


FIGURE A.2, SHEET 1

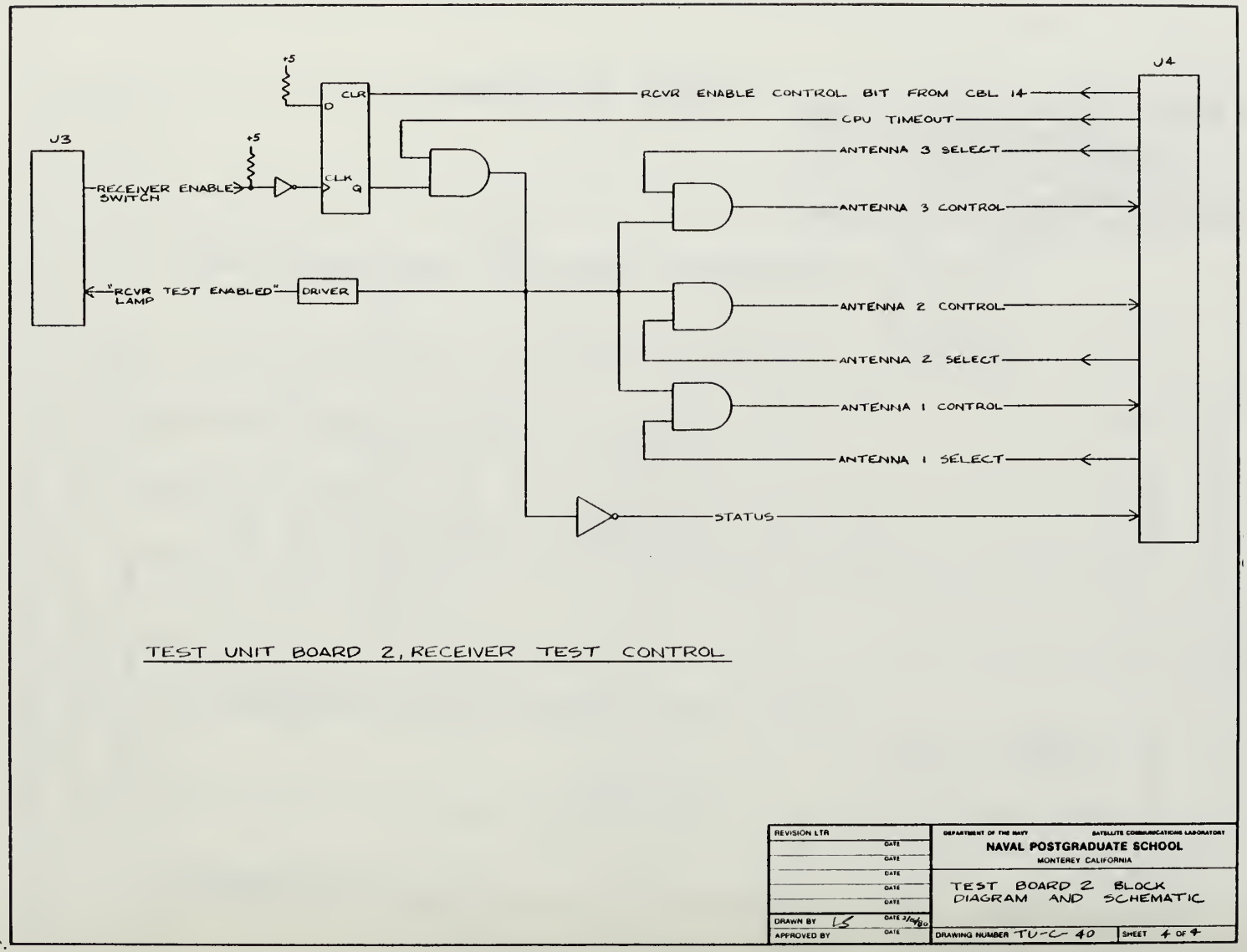


FIGURE A.2, SHEET 2

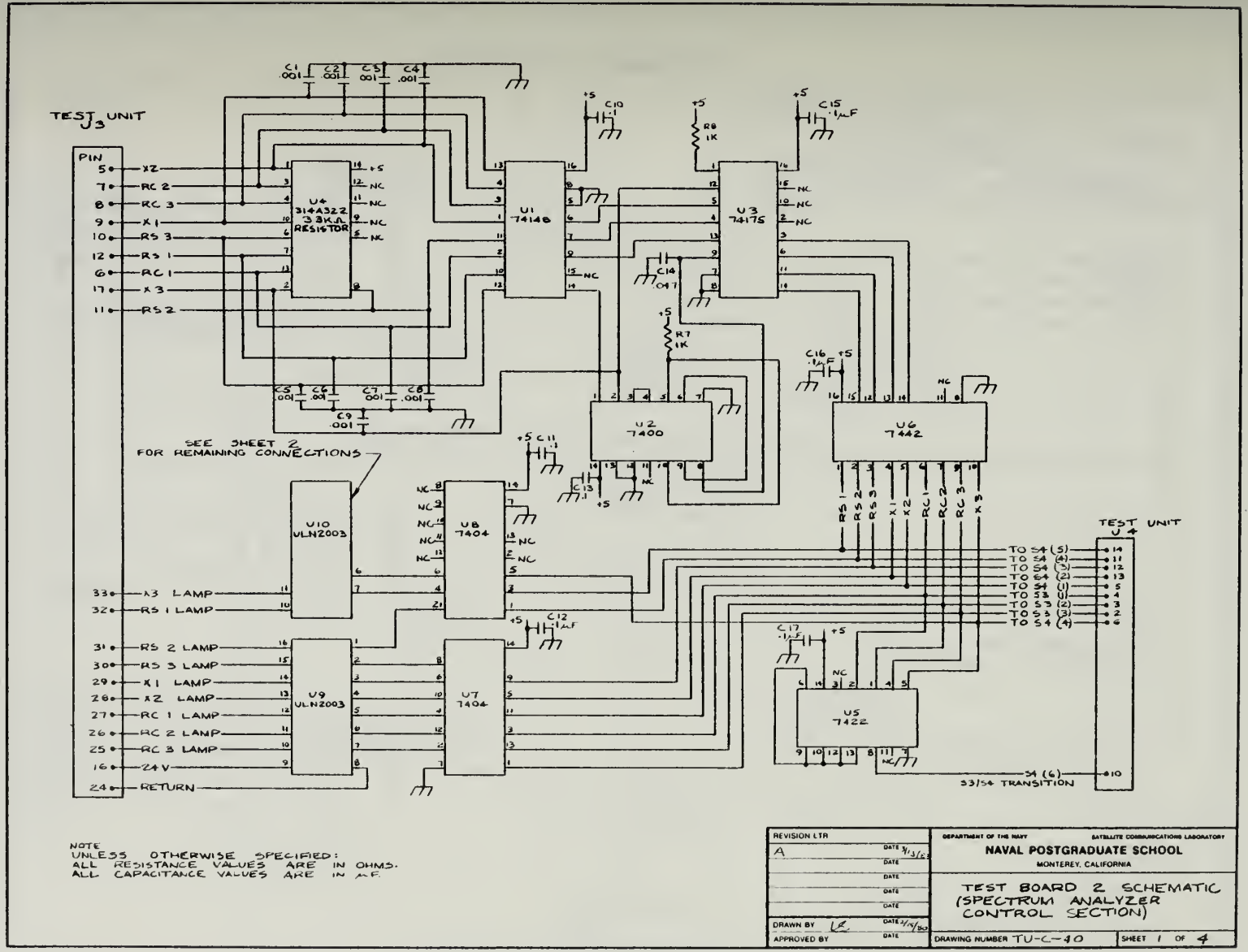


FIGURE A.2, SHEET 3

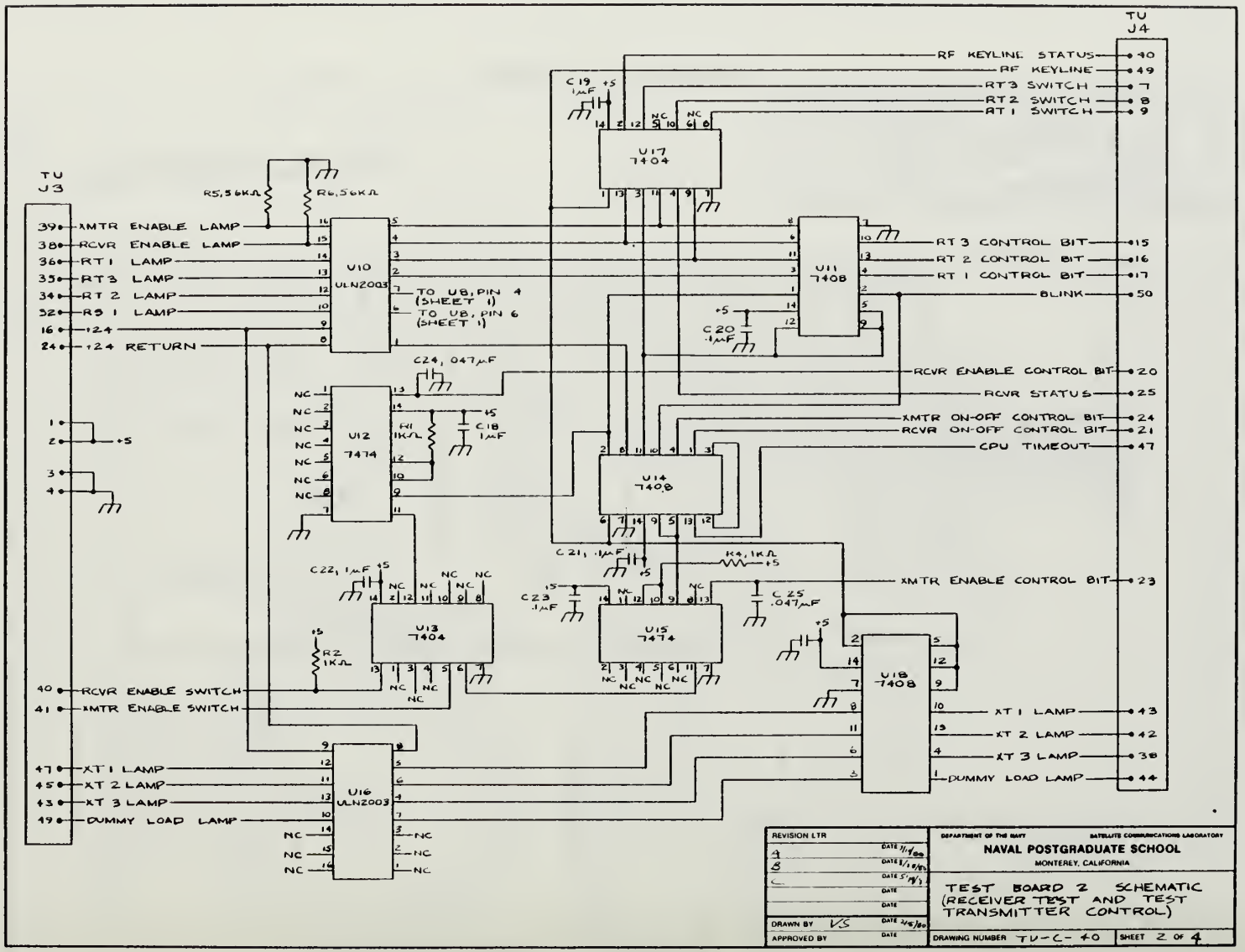


FIGURE A.2, SHEET 4

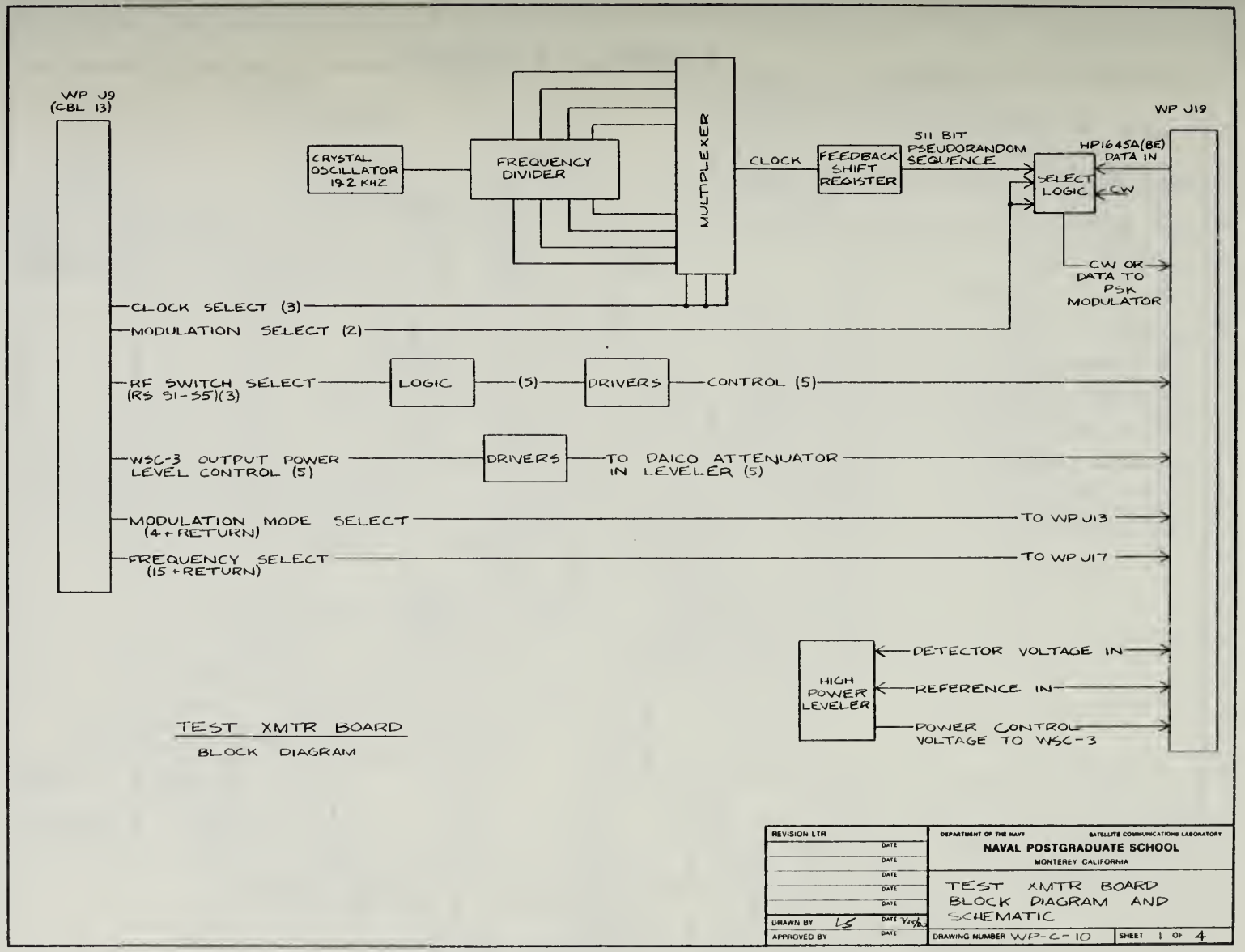


FIGURE A.3, SHEET 1

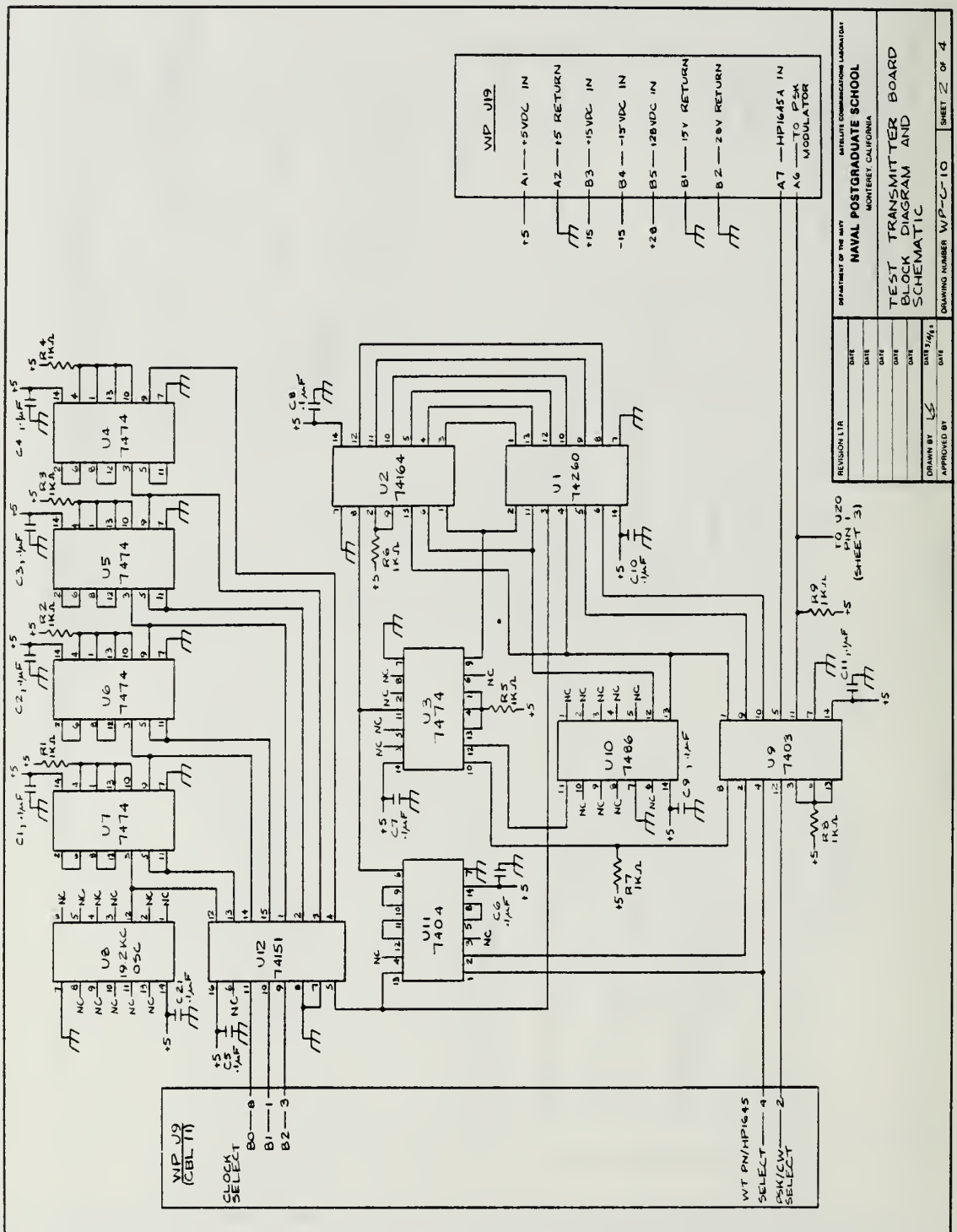


FIGURE A.3, SHEET 2

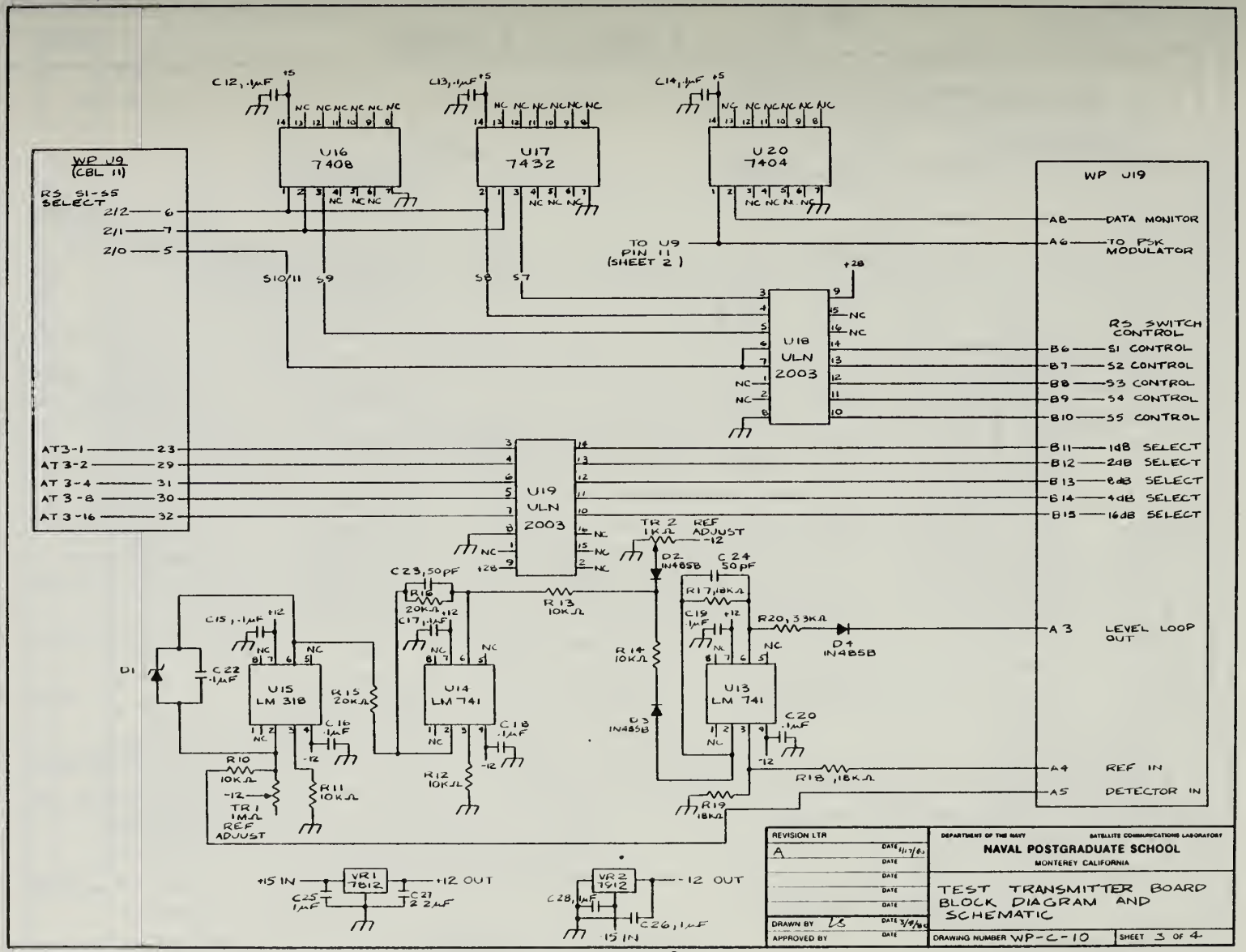


FIGURE A.3, SHEET 3

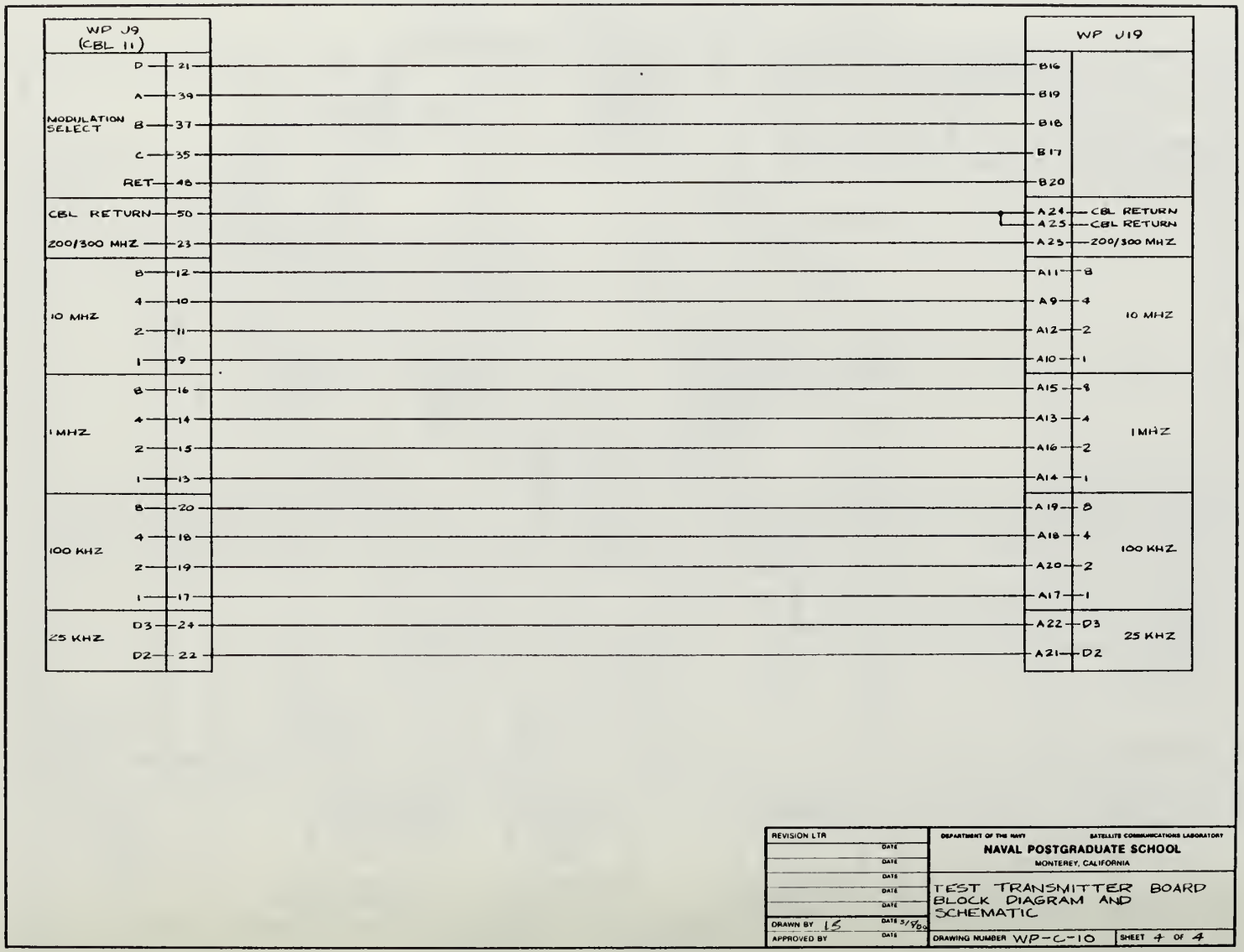


FIGURE A.3, SHEET 4

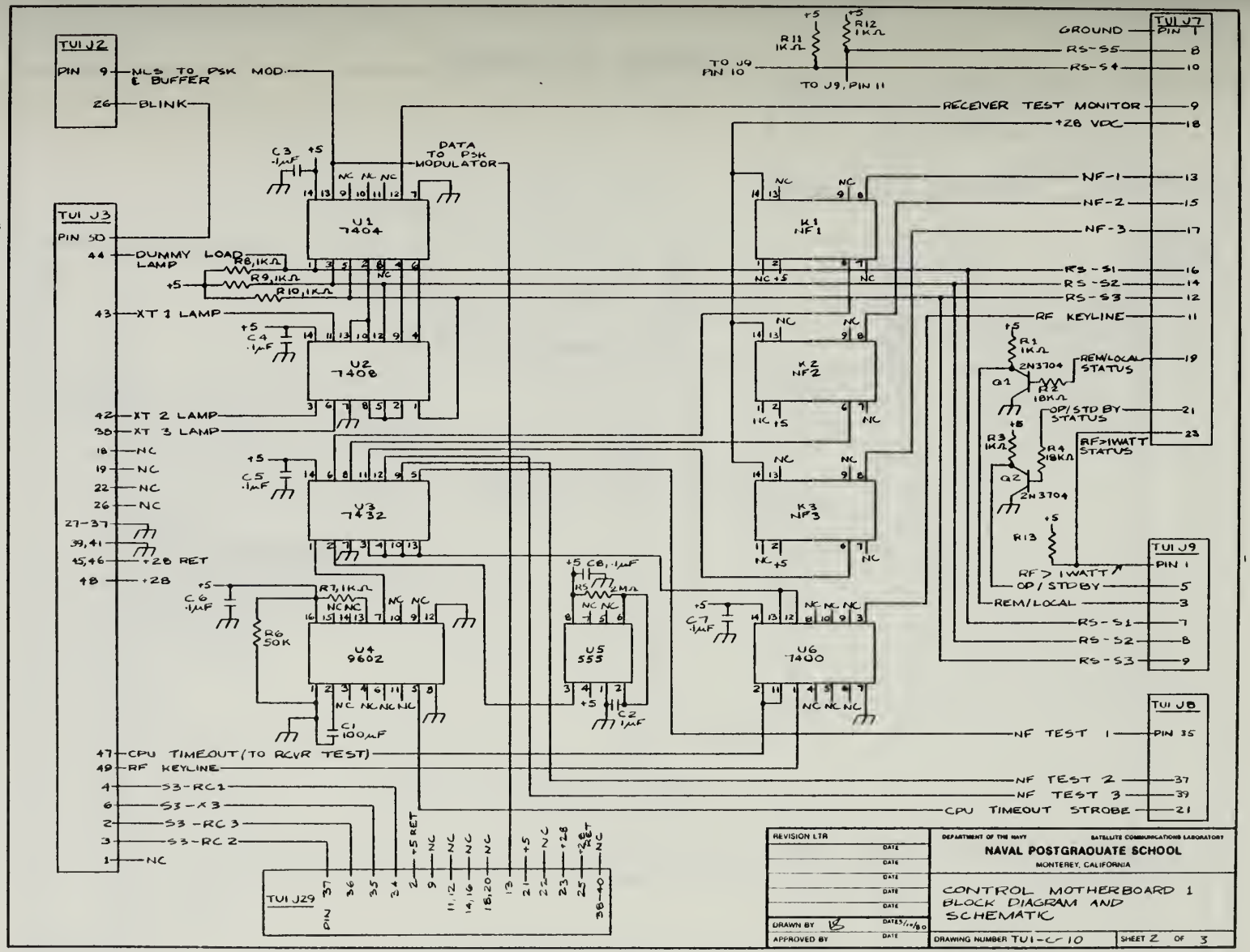


FIGURE A.4, SHEET 1

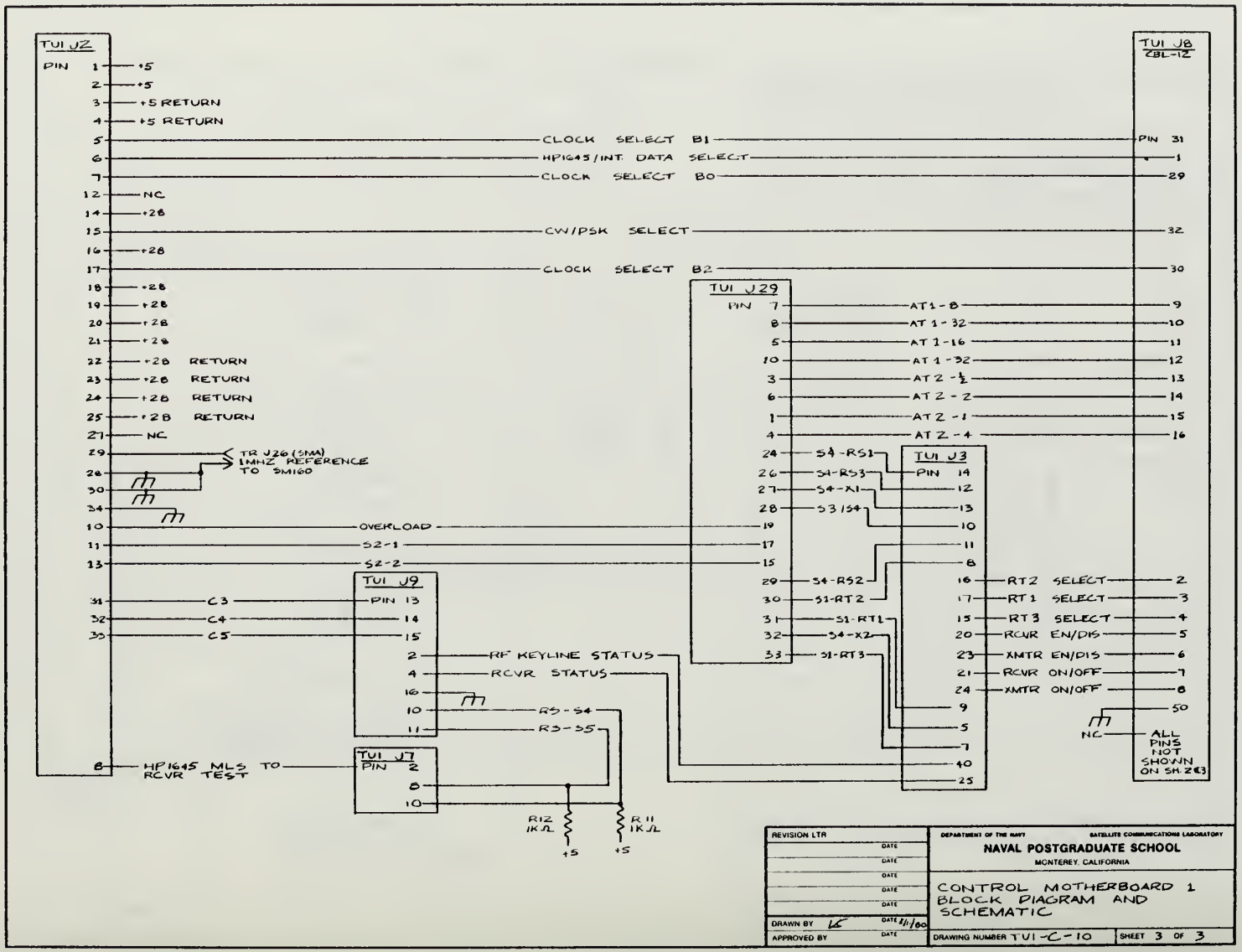


FIGURE A.4, SHEET 2

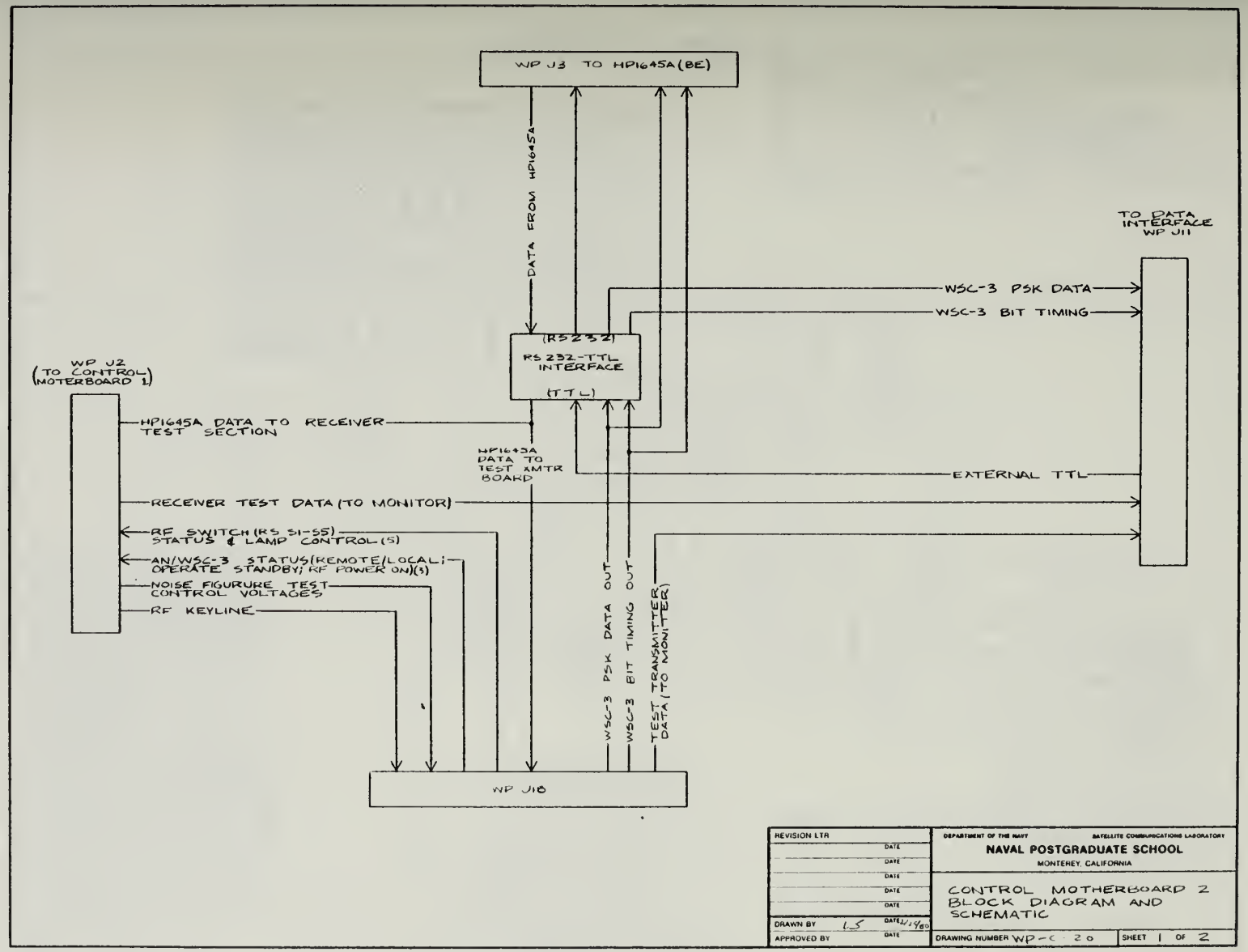


FIGURE A.5, SHEET 1

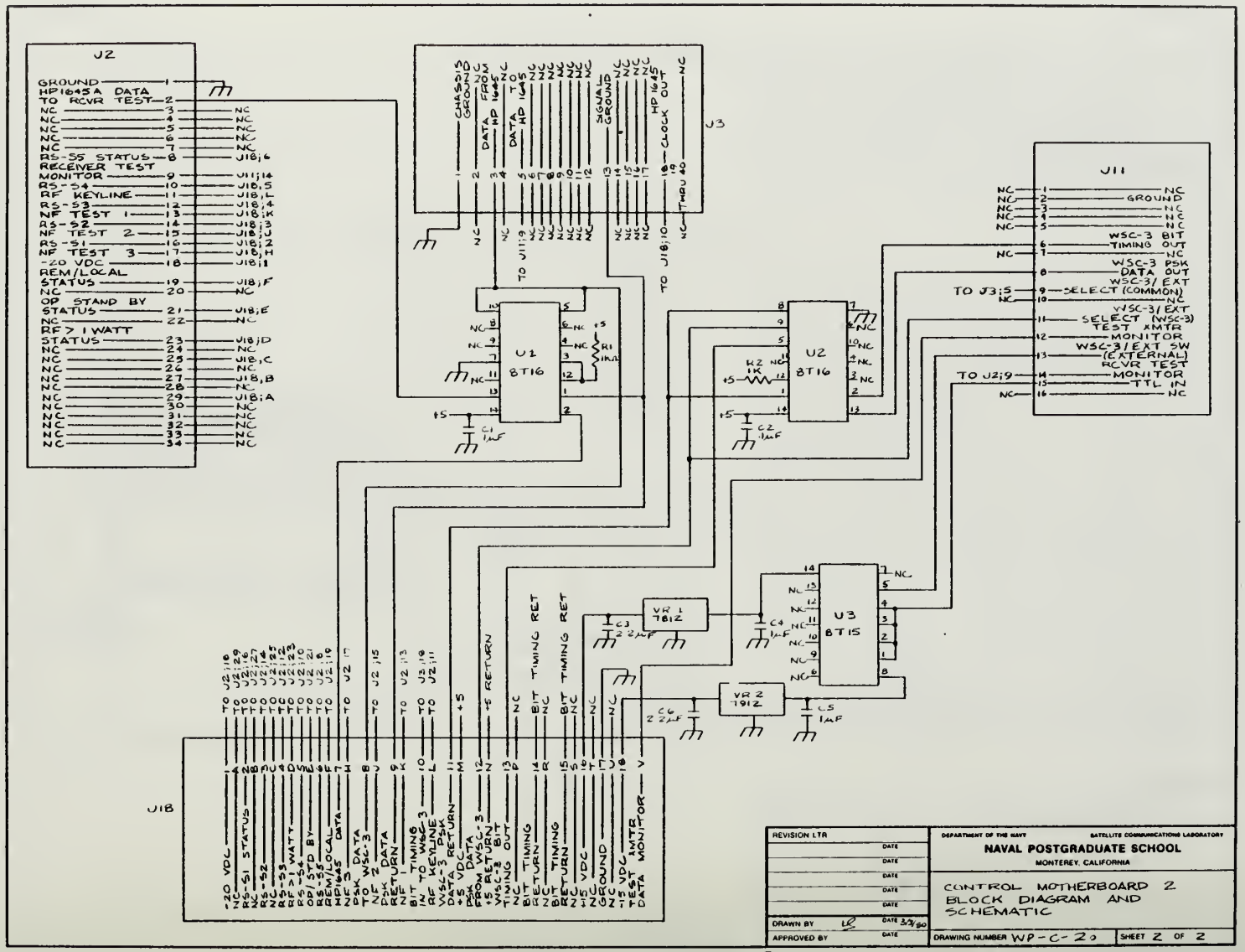
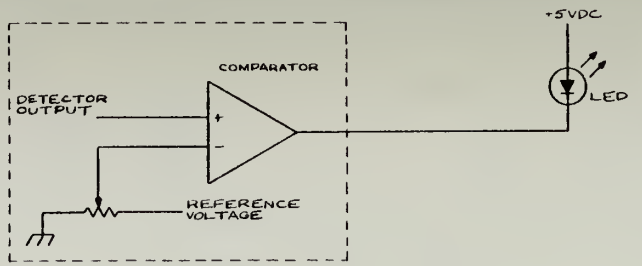
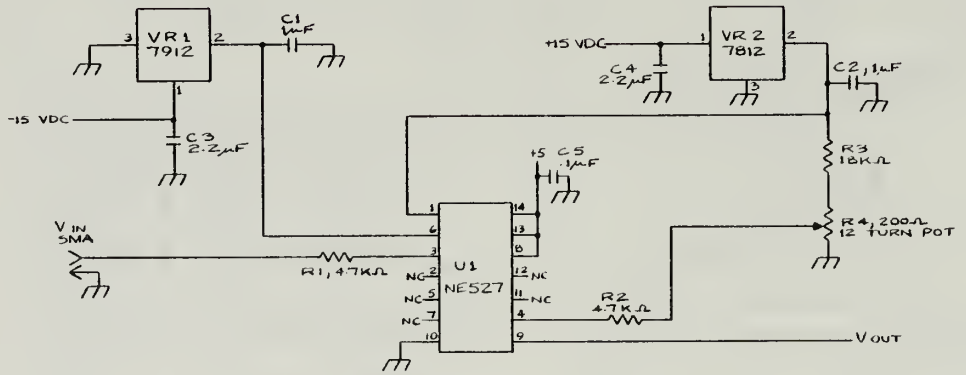


FIGURE A.5, SHEET 2



OVERLOAD DETECTOR
BLOCK DIAGRAM



OVERLOAD DETECTOR
SCHEMATIC

REVISION LTR		DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY
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	DATE	OVERLOAD DETECTOR
	DATE	BLOCK DIAGRAM AND SCHEMATIC
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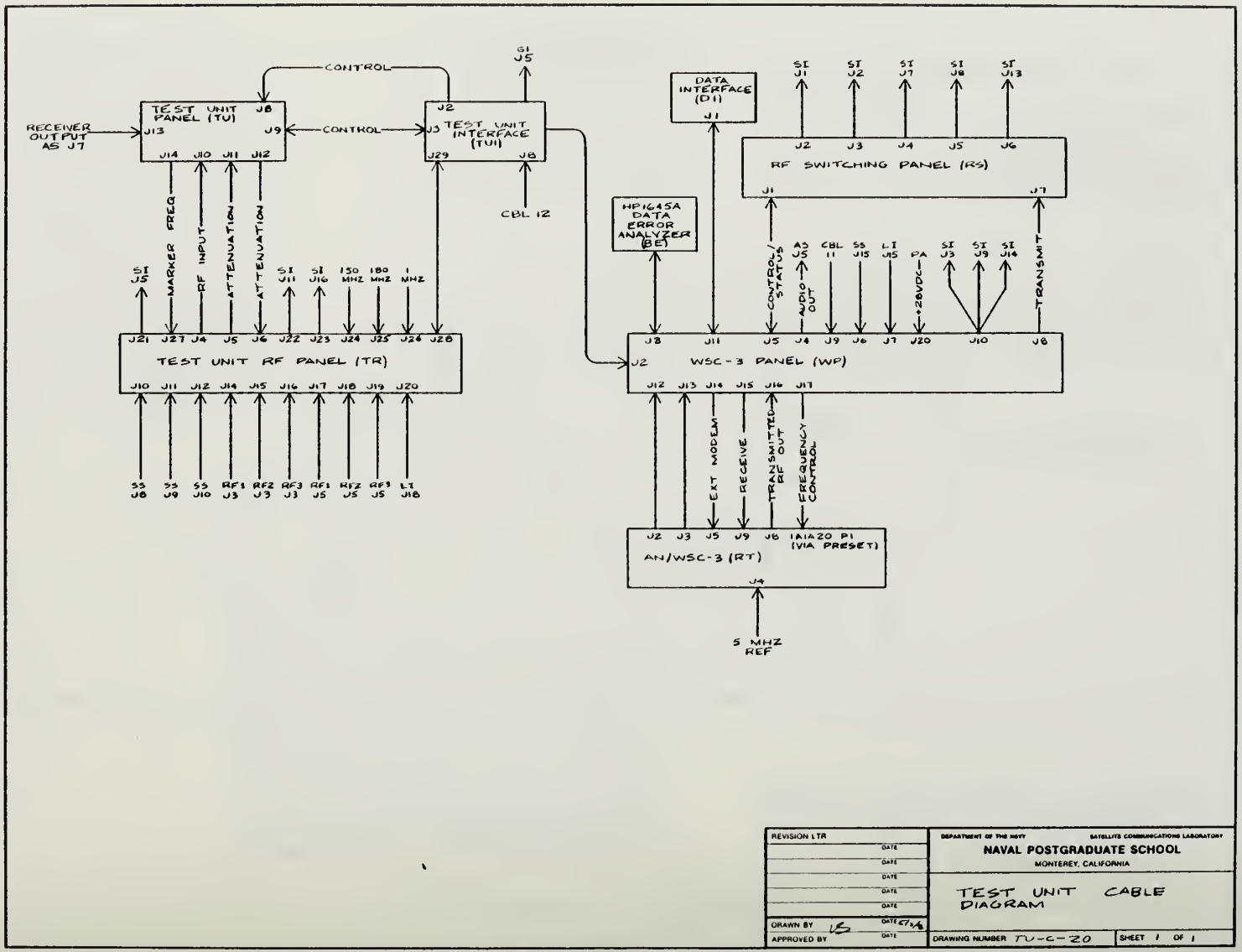
APPROVED BY	DATE	DRAWING NUMBER TR-C-20 — SHEET 1 OF 1

FIGURE A.6


TEST UNIT PANEL (TU)
RECEIVER OUTPUT AS J7
CONTROL
TEST UNIT INTERFACE (TUI)
CBL 12
DATA INTERFACE (DI)
HP1645A DATA ERROR ANALYZER (BE)
RF SWITCHING PANEL (RS)
TRANSMIT
TEST UNIT RF PANEL (TR)
WSC-3 PANEL (WP)
EXT MODEM
RECEIVE
TRANSMITTED RF OUT
FREQUENCY CONTROL
AN/WSC-3 (RT)
5 MHZ REF
FREQ
MARKER
RF INPUT
ATTENUATION
ATTENUATION
150 MHZ
180 MHZ
1 MHZ
AUDIO OUT
+28VDC
PA
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DRAWN BY
APPROVED BY
DEPARTMENT OF THE NAVY
SATELLITE COMMUNICATIONS LABORATORY
NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA
TEST UNIT CABLE DIAGRAM
DRAWING NUMBER TU-C-20
SHEET 1 OF 1

FIGURE A.7

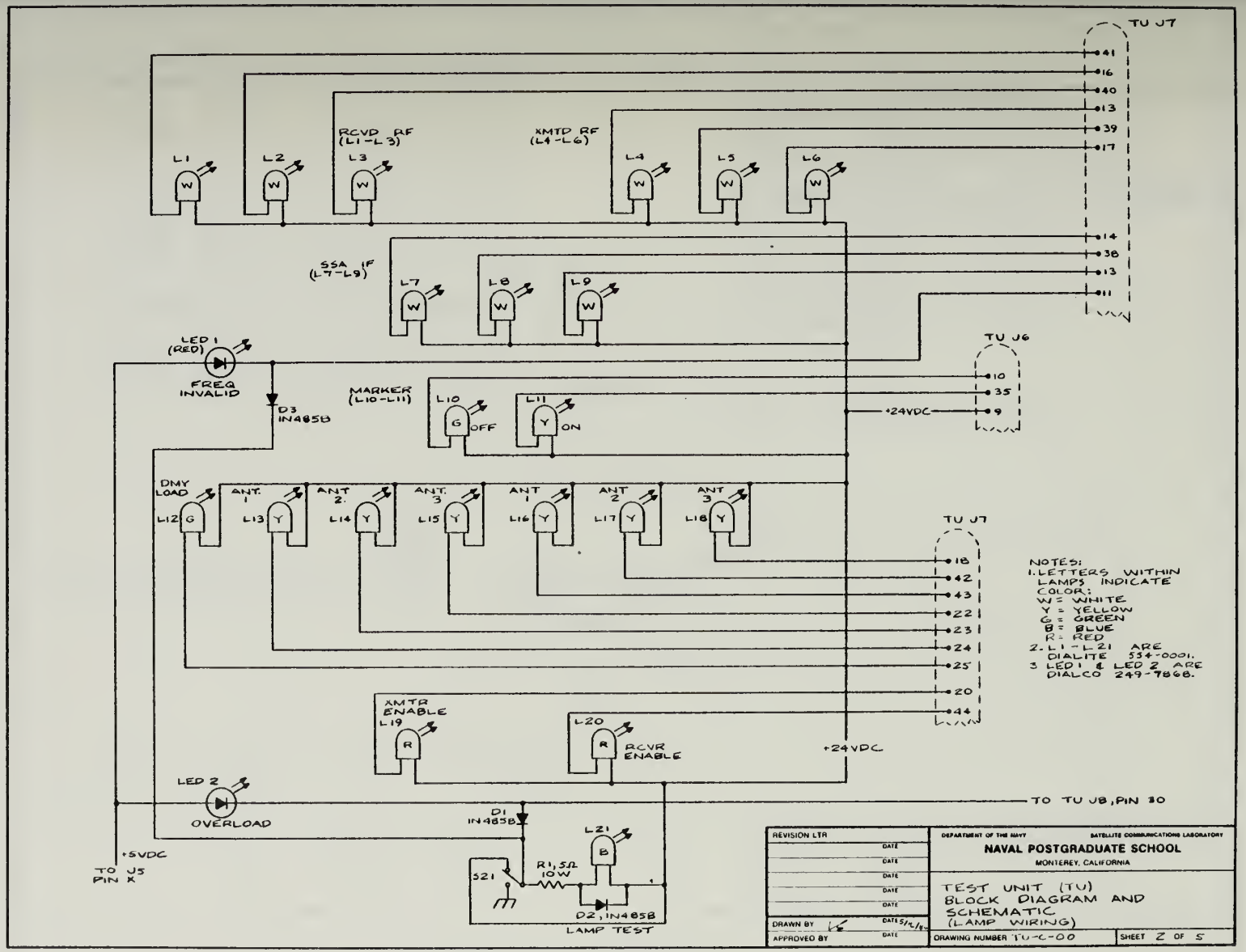


FIGURE A.8, SHEET 1

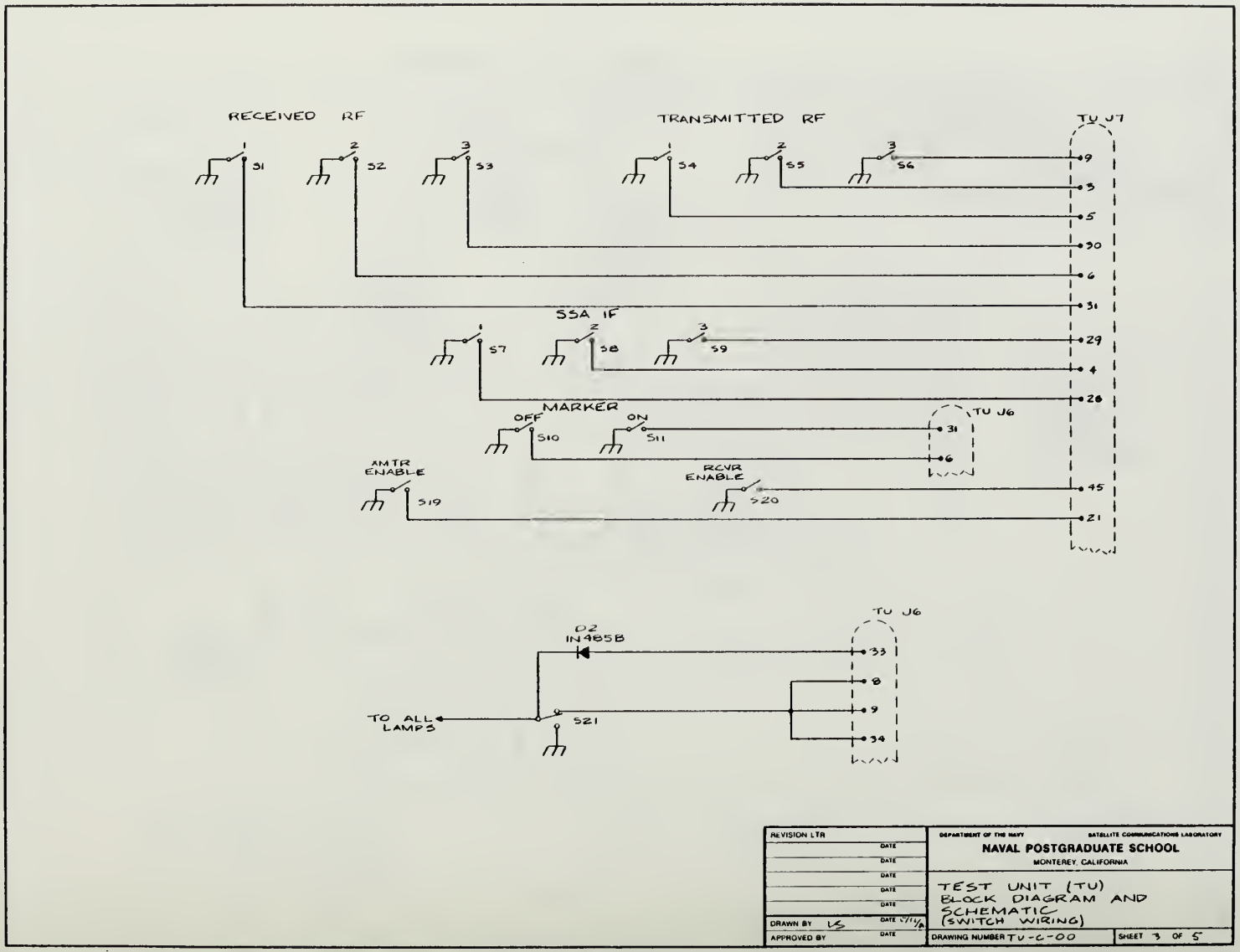


FIGURE A.8, SHEET 2

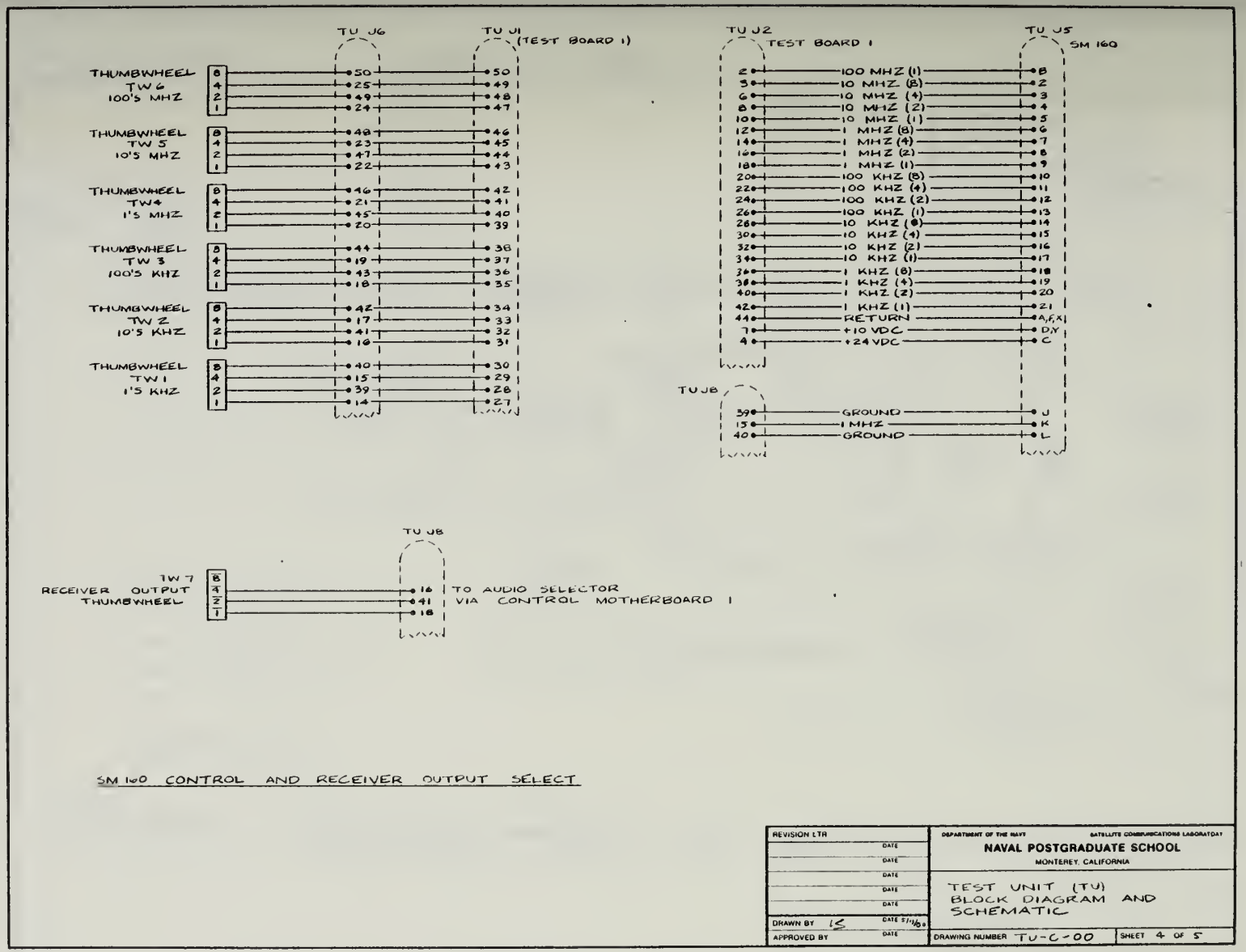
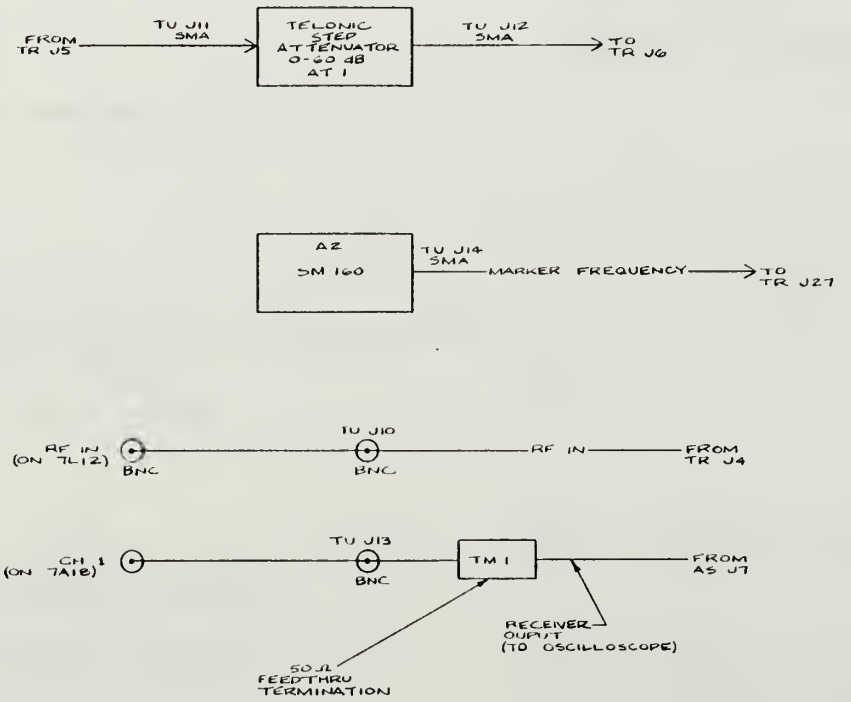


FIGURE A.8, SHEET 3



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APPROVED BY	DATE

DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY
NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA

TEST UNIT (TU) BLOCK DIAGRAM AND SCHEMATIC (RF SIGNAL ROUTING)

DRAWING NUMBER TU-C-00 — SHEET 5 OF 5

FIGURE A.8, SHEET 4

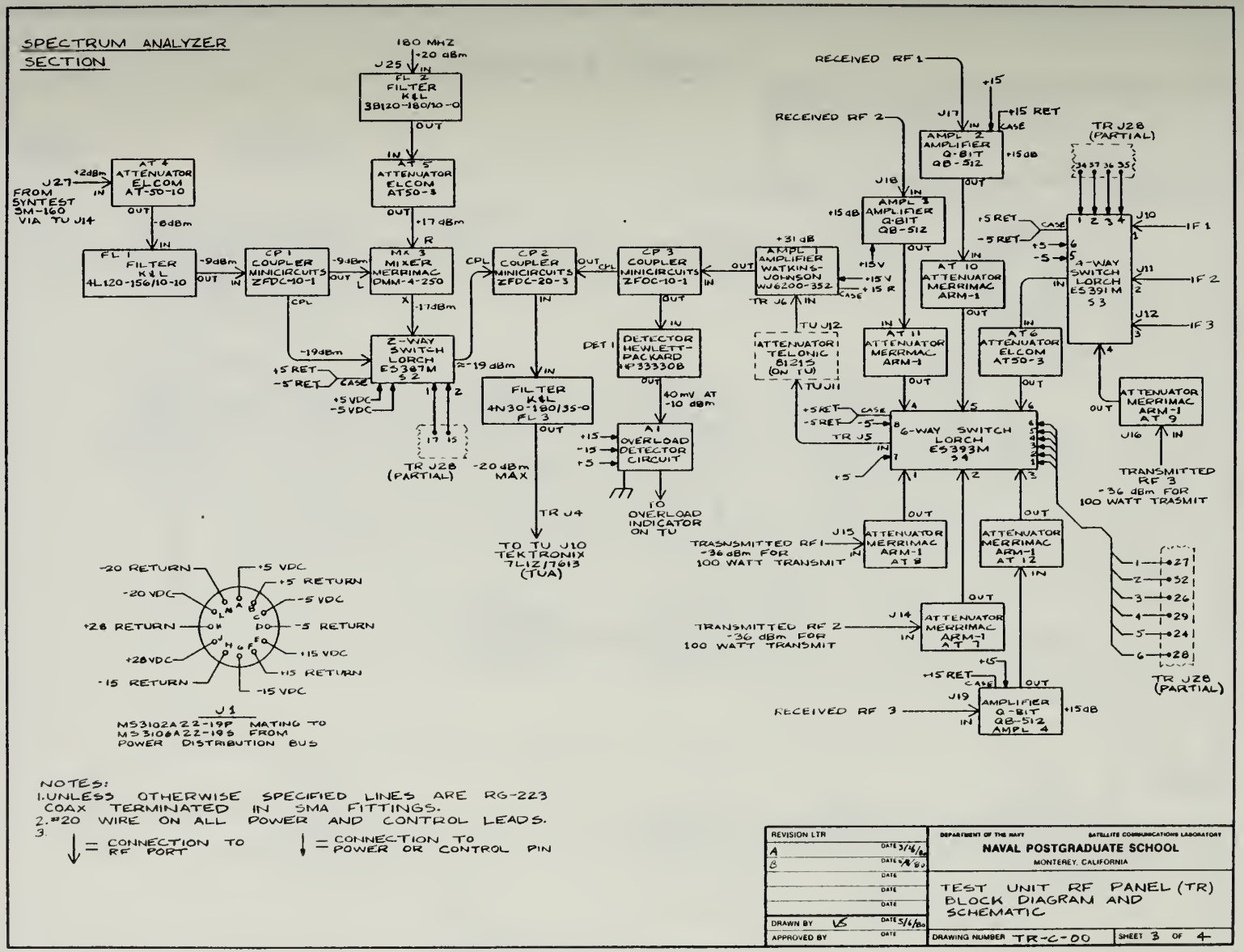


FIGURE A.9, SHEET 1

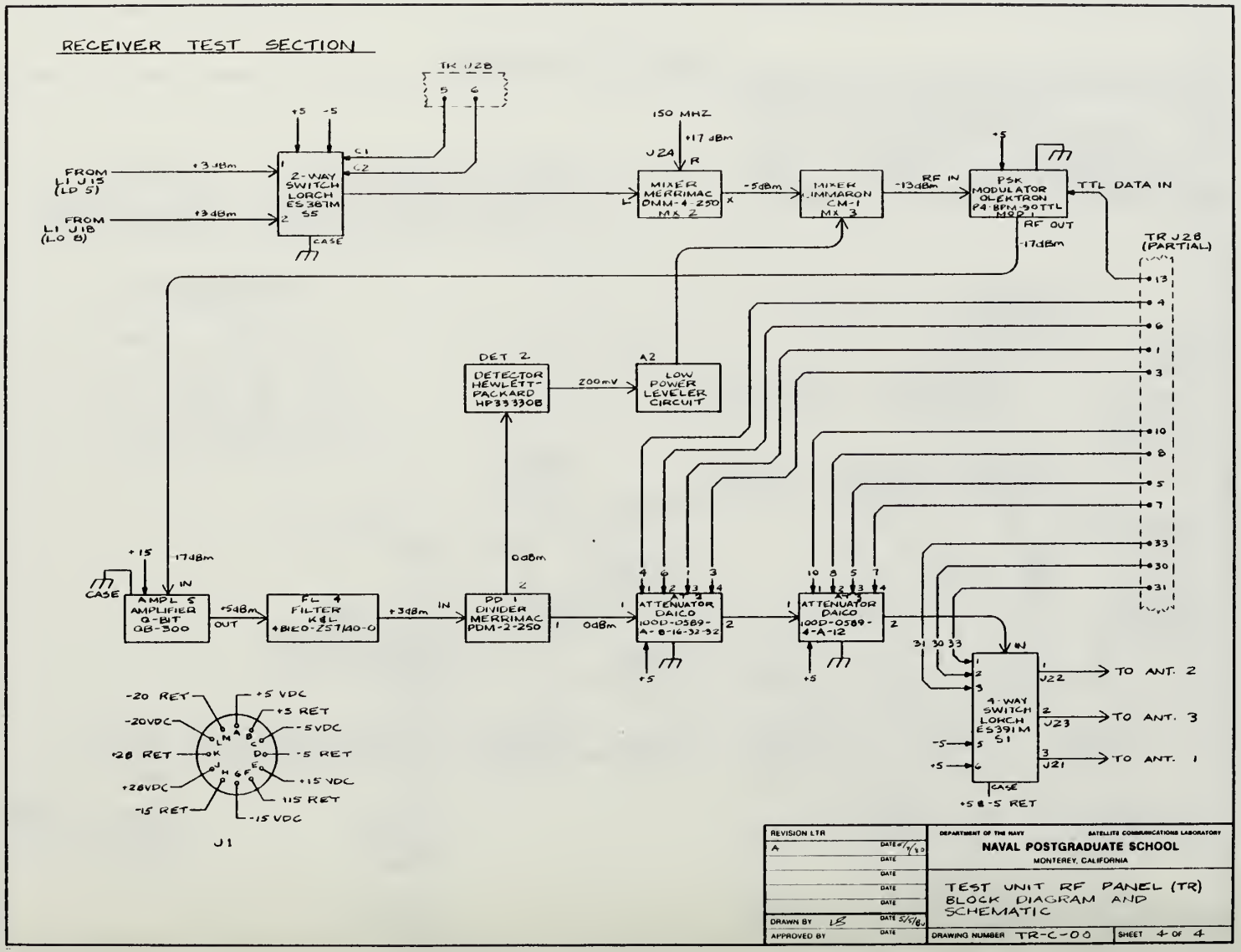


FIGURE A.9, SHEET 2

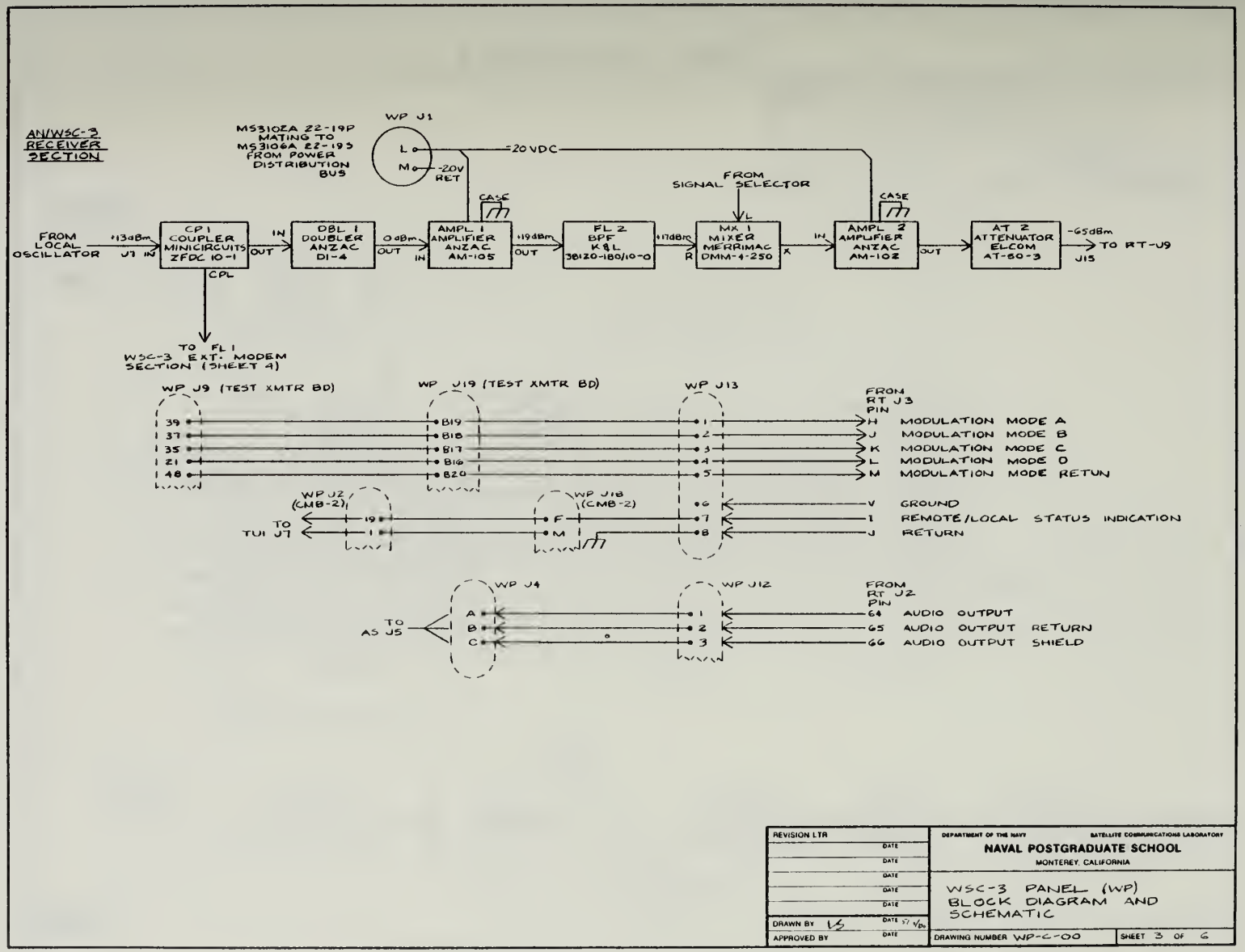
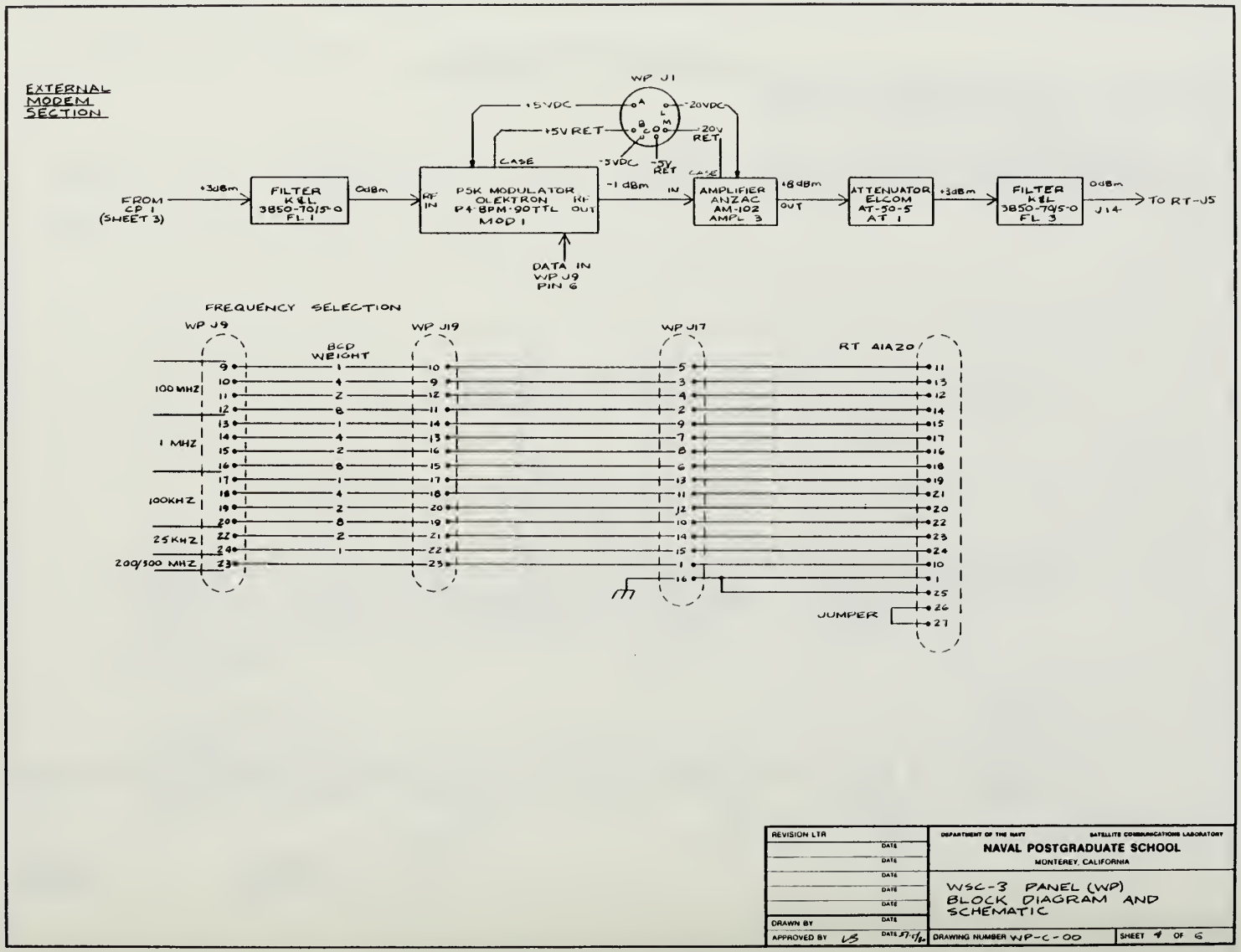


FIGURE A.10, SHEET 1



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APPROVED BY LS	DATE 5/16

DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY
NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA

WSC-3 PANEL (WP) BLOCK DIAGRAM AND SCHEMATIC

DRAWING NUMBER WP-C-00 — SHEET 4 OF 6

FIGURE A.10, SHEET 2

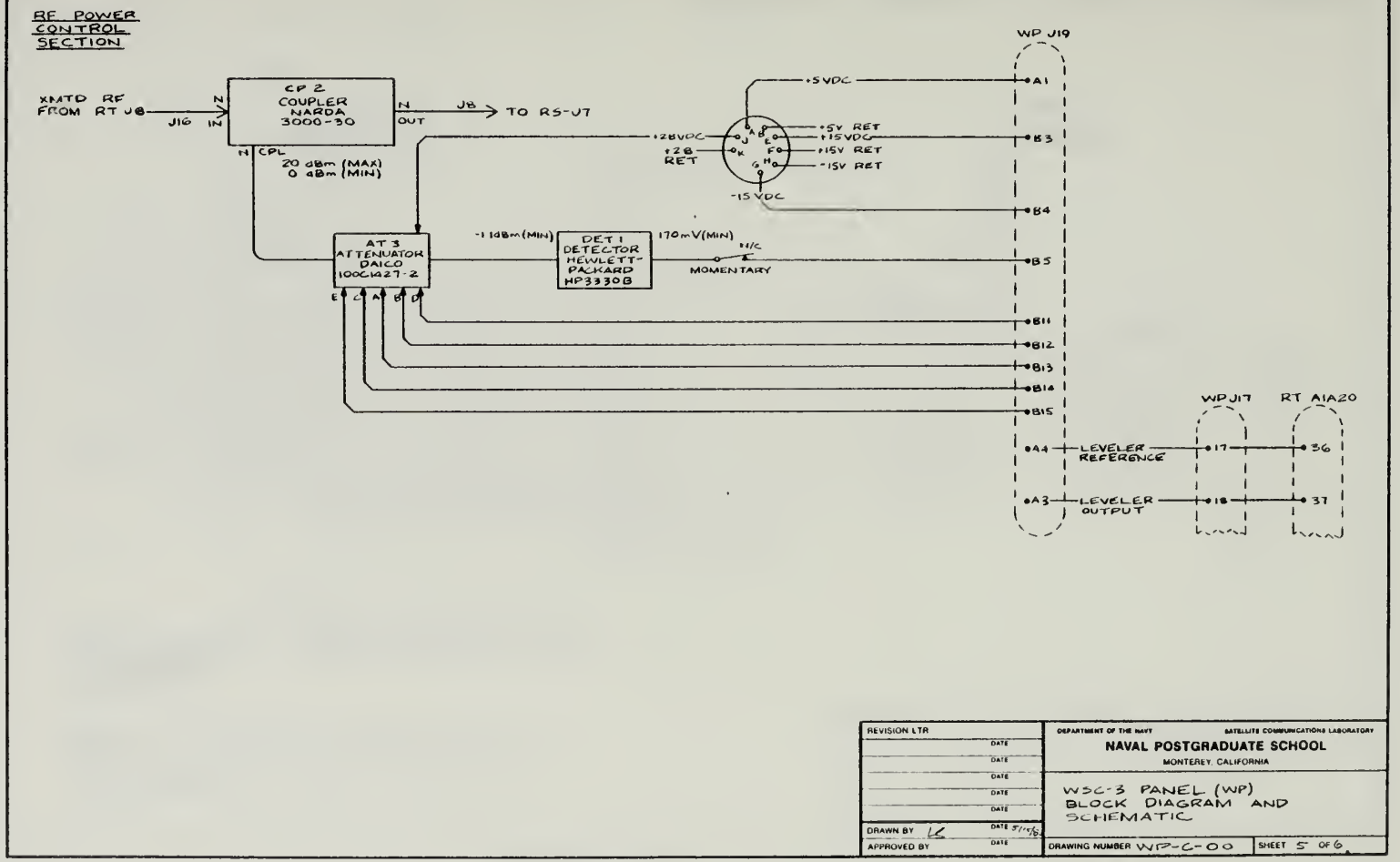


FIGURE A.10, SHEET 3

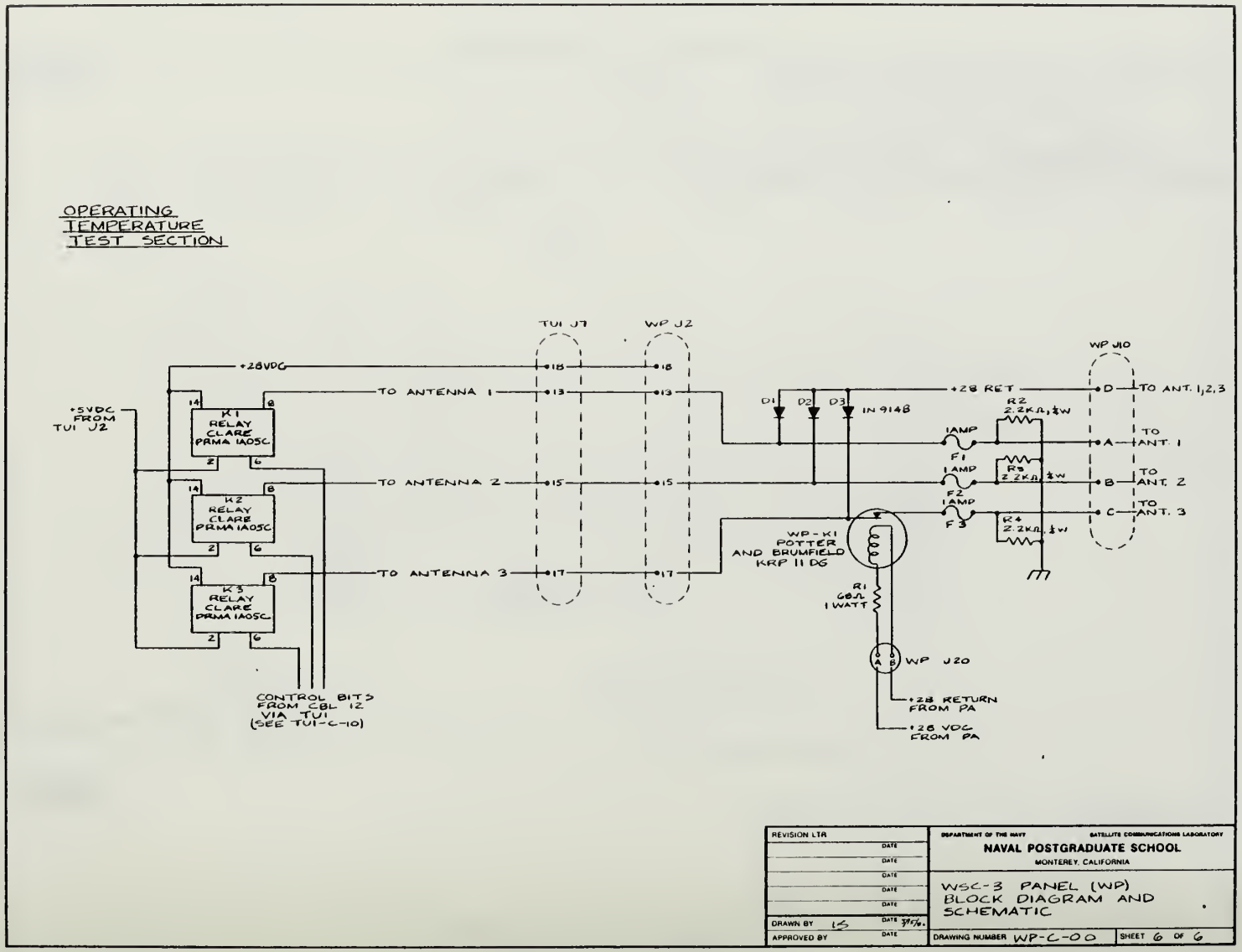
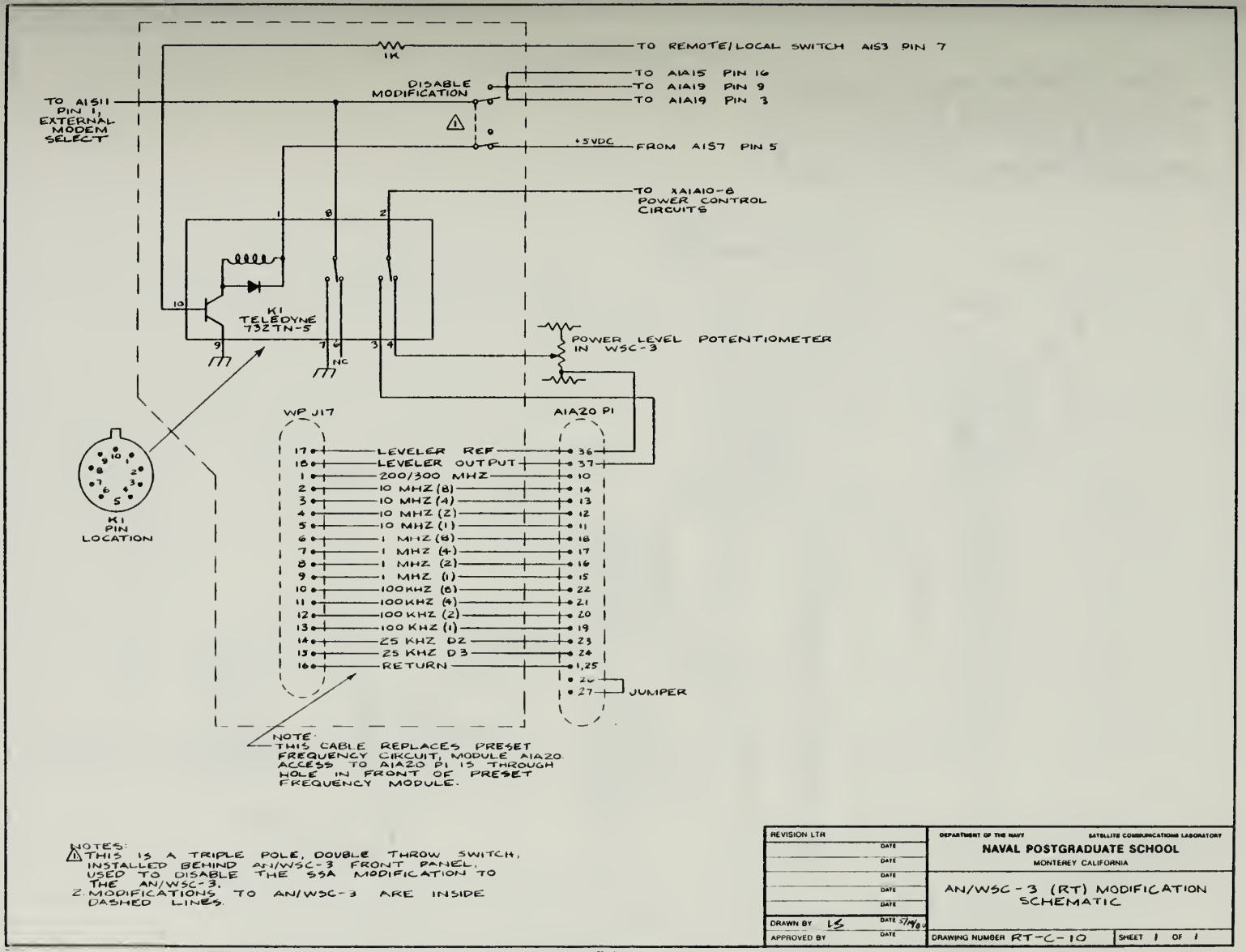


FIGURE A.10, SHEET 4



NOTES:
1. THIS IS A TRIPLE POLE, DOUBLE THROW SWITCH, INSTALLED BEHIND AN/WSC-3 FRONT PANEL, USED TO DISABLE THE SSA MODIFICATION TO THE AN/WSC-3.
2. MODIFICATIONS TO AN/WSC-3 ARE INSIDE DASHED LINES.

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APPROVED BY	DATE

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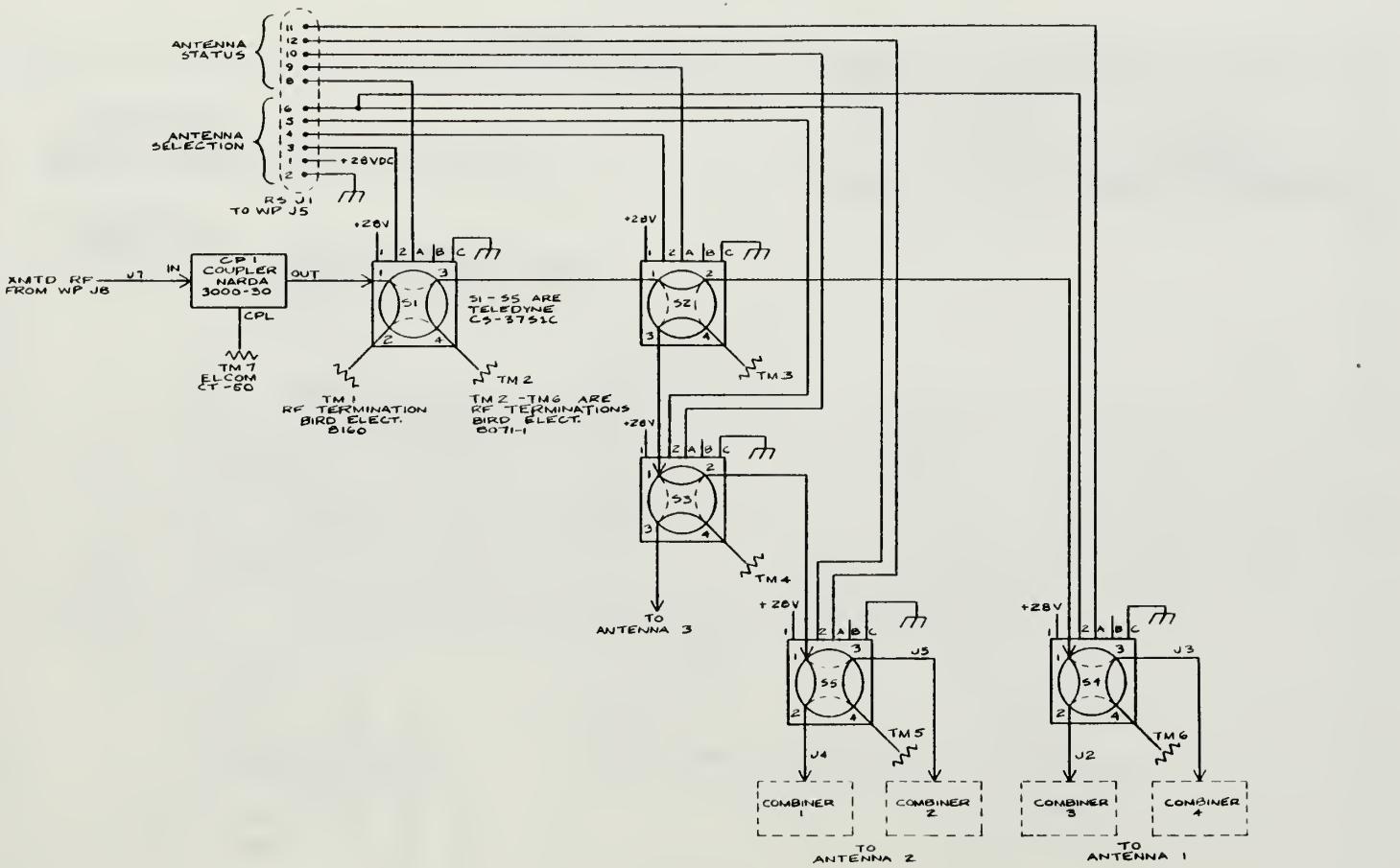
AN/WSC-3 (RT) MODIFICATION SCHEMATIC

DRAWING NUMBER RT-C-10 — SHEET 1 OF 1

FIGURE A.11



REVISION LTR	DATE	DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY
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		MONTEREY, CALIFORNIA
		RF SWITCHING PANEL (RS) BLOCK DIAGRAM AND SCHEMATIC
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APPROVED BY	DATE	DRAWING NUMBER RS-C-00 — SHEET 2 OF 2

FIGURE A.12

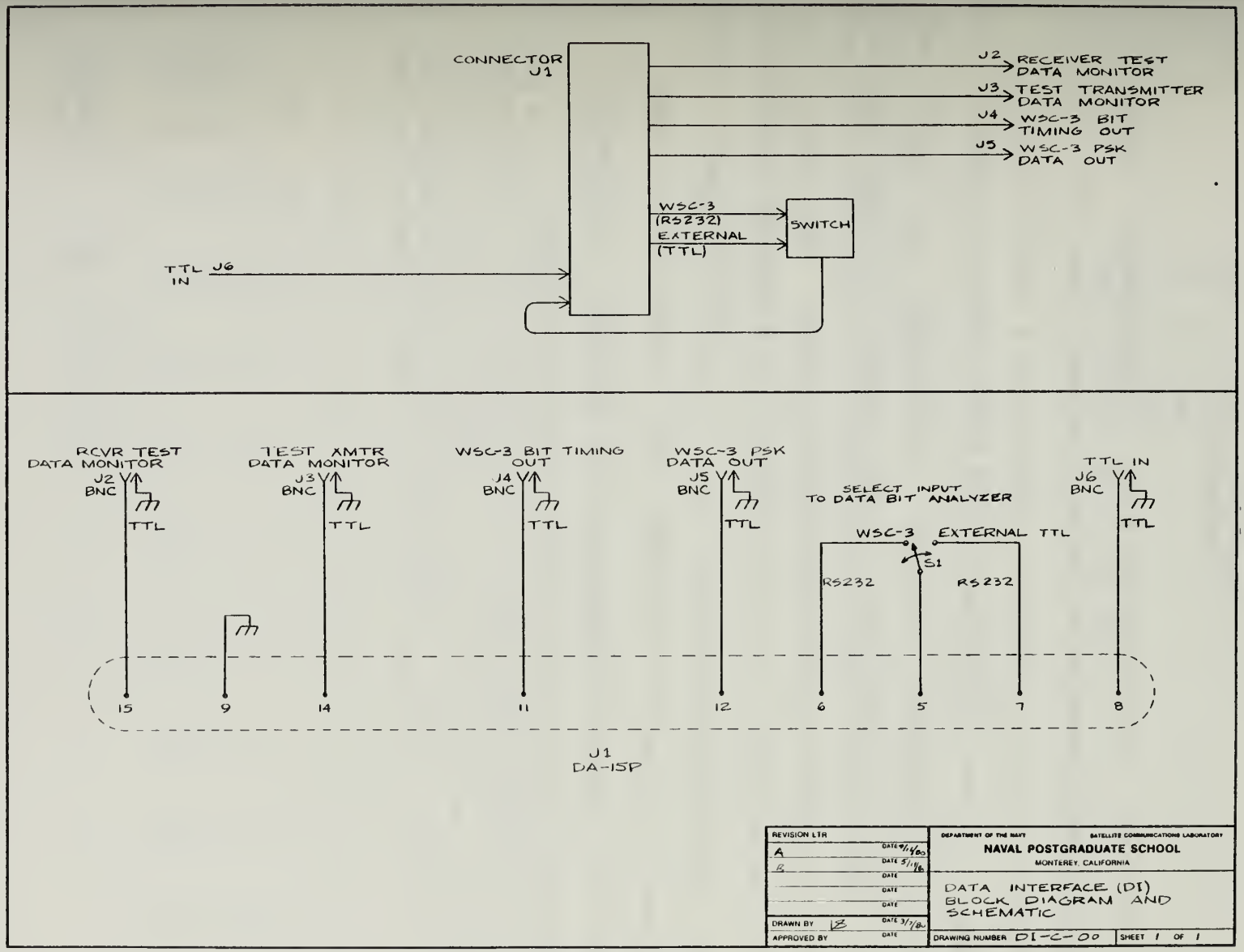
CONNECTOR J1
J2 RECEIVER TEST DATA MONITOR
J3 TEST TRANSMITTER DATA MONITOR
J4 WSC-3 BIT TIMING OUT
J5 WSC-3 PSK DATA OUT
WSC-3 (RS232) EXTERNAL (TTL)
SWITCH
TTL J6 IN
RCVR TEST DATA MONITOR
J2 BNC
TTL
TEST AMTR DATA MONITOR
J3 BNC
TTL
WSC-3 BIT TIMING OUT
J4 BNC
TTL
WSC-3 PSK DATA OUT
J5 BNC
TTL
SELECT INPUT TO DATA BIT ANALYZER
WSC-3 EXTERNAL TTL
S1
RS232
RS232
TTL IN
J6 BNC
TTL
15
9
14
11
12
6
5
7
8
J1
DA-15P
REVISION LTR
A DATE 7/1/80
B DATE 5/1/81
DRAWN BY DATE 3/1/81
APPROVED BY DATE
DEPARTMENT OF THE NAVY SATELLITE COMMUNICATIONS LABORATORY
NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA
DATA INTERFACE (DI) BLOCK DIAGRAM AND SCHEMATIC
DRAWING NUMBER DI-C-00
SHEET 1 OF 1

FIGURE A.13

APPENDIX B

CONTROL BUS

The SSA is controlled by a PDP 11-34 computer. This machine communicates with the SSA via the Control Bus. A portion of the bus provides an address of a specific sub-system; the remainder makes up the actual control signal. Each SSA sub-system is assigned a Control Bus Latch Board (CBL). The CBL latches any control signals that appear on the Control Bus for its corresponding system. CBL11 and CBL12 are assigned to the TEST UNIT. Bit assignments for CBL11 and CBL12 are listed on the following two pages. Information as to CBL assignment, pin connections and local oscillator frequency control is also provided. Reference 1 describes in detail the digital control of the SSA.

A. Control Bus Latch Board Assignments:

Board number = device address = CB chassis slot number

1-8:	LO1 through LO8, respectively
9-10:	SS (controlling SRs and FRs, respectively)
11:	RT (via WP)
12:	TU (via TUI)
13:	FR1 and FR2 (via RI)
14:	SR1 through SR4 (via RI)
15:	AD1 through AD4 and Miscellaneous (via CI)

B. CCP (DR11-C) Output Data Register format:

The data byte is transmitted in bits 15 through 8 (LSB);
bits 7 and 6 are unused;
CBL board number is transmitted in bits 5 through 2;
the data byte number is transmitted in bits 1 and 0 (LSB).

Throughout, bit 0 is the LSB and byte 0 is the LSByte
(where this concept is relevant).

Logic: positive-true

C. CBL 50-pin Connector pin assignments:

One end of a CBL cable will be a 50-pin edge connector; the other end will be EITHER another 50-pin edge connector OR a 50-pin microribbon connector. In either case, pin 1 of one connector will be connected to pin 1 of the other connector (via the edge wire of the flat cable). The pin numbering of the two connector types is different, however:

1) Pin numbers on 50-pin edge connector (at CBL,TR and WP)

bit:	ND+	ND-	7	6	5	4	3	2	1	0 (LSB)
Byte 3:	36	26	32	30	31	29	39	37	35	33
Byte 2:	38	25	4	2	3	1	8	6	7	5
Byte 1:	40	28	12	10	11	9	16	14	15	13
Byte 0:	46	27	20	18	19	17	24	22	23	21

Vcc (+5V): 42, 44, 45, 47, 49
Ground: 34, 41, 48, 50
Unused: 43

Logic: negative-true

2) Pin numbers on 50-pin microribbon connector (at CI,LO,RI and SS)

bit:	ND+	ND-	7	6	5	4	3	2	1	0 (LSB)
Byte 3:	43	38	41	40	16	15	20	19	18	17
Byte 2:	44	13	27	26	2	1	29	28	4	3
Byte 1:	45	39	31	30	6	5	33	32	8	7
Byte 0:	48	14	35	34	10	9	37	36	12	11

Vcc (+5V): 23, 24, 25, 46, 47
Ground: 21, 42, 49, 50
Unused: 22

ND+ = New Data+ : Positive-going edge can be used to clock in new data.
ND- = New Data- : Negative-going edge can be used to clock in new data.

D. Logic for specific Control Bus Latch Boards.

Positive-true logic: +5V means TRUE, ON, or binary 1.
Negative-true logic: 0V means TRUE, ON, or binary 1.

CBL1 through CBL8 (L01 through L08):

Byte 3:
bits 7-4: 10s of MHz (hexadecimal)
bits 3-0: MHz (BCD)

Byte 2:
bits 7-4: 100s of kHz (BCD)
bits 3-0: 10s of kHz (BCD)

Byte 1:
bits 7-4: kHz (BCD)
bits 3-0: 100s of Hz (BCD)

Byte 0:
bits 7-4: 10s of Hz (BCD)
bits 3-0: Hz (BCD) (has no effect on present version of LO)

Logic: negative-true

CBL12 (TU):

Byte 3:

bit 7: select PSK (vice CW)
bits 6-4: internal PSK clock rate:
7 = 19.2 KHz, 6 = 9600 Hz, 5 = 4800 Hz,
4 = 2400 Hz, 3 = 1200 Hz, 2 = 600 Hz,
1 = 300 Hz, 0 = 75 Hz
bit 3: disable noise diode feeding RF3 (normally disabled)
bit 2: disable noise diode feeding RF2 (normally disabled)
bit 1: disable noise diode feeding RF1 (normally disabled)
bit 0: select L08 (vice L05) for Test Unit

Logic: positive-true

Byte 2:

bit 7: select AN3 for receiver test signal
bit 6: select AN2 for receiver test signal
bit 5: select AN1 for receiver test signal
N.B. The three bits above are mutually exclusive. Only one antenna can get receiver test signal at a time.
bit 4: select HP1645's PSK data (vice internal PSK data)
bit 3: RT transmitter on
bit 2: RT transmitter enable
N.B.: Operator must push XMTR ENABLE on TU in addition to bits 2 and 3 being on, to start test.
bit 1: receiver test on
bit 0: receiver test enable
N.B.: Operator must push RCVR ENABLE on TU in addition to bits 0 and 1 being on, to start test.

Logic: positive-true

Byte 1:

bit 7: 32 dB of attenuation for receiver test signal (use only when bits 6-0 are insufficient)
bits 6-0: attenuation for receiver test signal, in units of 0.5 dB

Logic: negative-true

Byte 0:
bits 7-1: unused
bit 0: CPU timeout (pulse at 1 pps) - purpose is to shut down XMTR if CPU fails

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CBL11 (RT): (AN/WSC-3 control via WP)

Byte 3:
bits 7-3: attenuation for RT transmitter, in units of 1 dB (range is 0-20 dB; must not be permitted to exceed 20dB)
bits 2-0: non-AM modulation select;
0 = FM, 1 = FSK, 2 = PSK/9600 baud, 3 = PSK/4800 buad, 4 = PSK/2400 baud, 5 = PSK/1200 baud, 6 = PSK/300 baud, 7 = PSK/75 baud or AM (see byte 0 below)

Logic: positive-true

Byte 2:
bit 7: select HP1645's PSK data (vice internal PSK data)
bit 6: select PSK (vice CW)
bits 5-3: internal PSK clock rate:
7 = 19.2 kHz, 6 = 9600 Hz, 5 = 4800 Hz, 4 = 2400 Hz, 3 = 1200 Hz, 2 = 600 Hz, 1 = 300 Hz, 0 = 75 Hz
bits 2-1: antenna select for transmit:
3 = AN3, 2 = AN2, 1 = AN1, 0 = dummy load
bit 0: select combiner #2 (vice combiner #1)
(irrelevant if AN3 is selected)

Logic: positive-true

Byte 1: frequency selection
bits 7-4: 10's of MHz (BCD)
bits 3-0: MHz (BCD)

Logic: negative-true

Byte 0: frequency selection
bits 7-4: 100's of KHz (BCD)
bits 3-2: 25's of KHz (always zero - use L05 to tune less than 100 kHz)
bit 1: 300 MHz (vice 200 MHz)
bit 0: select AM modulation vice non-AM (see byte 3)

APPENDIX C

TESTING AND TROUBLESHOOTING

The procedures listed in this Appendix may be used to test the TEST UNIT for proper operation during installation and calibration, or to troubleshoot TEST UNIT components suspected of being faulty. Testing and troubleshooting procedures are given down to the module level (PC board, panel, assembly). If a module is found to have failed it is to be replaced within the SSA. Repairs are not normally made on location but are delivered to the appropriate repair facility.

I. RECEIVER TEST SECTION

A. SIGNAL SET-UP

Two means are available by which Receiver Test signals may be generated. The first and by far the most convenient is through use of the Touch Panel and the Interim Signal menu. By using this menu the operator is guided in the selection of power level, frequency, antenna and modulation, and the signal is set up automatically. If the Touch Panel is not used, the test signal must be set up manually. To do this, proceed as follows:

1. Replace CBL12 with a BIT-BOX at TUI J8. Select POSITIVE TRUE logic. (The BIT-BOX is a CBL simulator, consisting of 32 toggle switches whose outputs are TTL compatible.)

2. Replace CBL8 with a BIT-BOX at L08. Select NEGATIVE TRUE logic.

3. Determine the desired frequency in the range of 240-270 MHz. Subtract 150 MHz from the desired frequency. Using the BIT-BOX at L08, program the local oscillator to equal the difference found above.

4. Locate U4 on CMB-I at TUI. Jumper pin 7 of U4 to ground, in order to by-pass the CPU TIMEOUT strobe.

5. Using the BIT-BOX at TUI J8, select desired modulation. See Appendix B for a list of which bits of CBL12 control

modulation. Refer to Appendix B as needed during the remainder of this procedure.

6. Place all switches by Byte 1 in the LOW position. Byte 1 selects attenuation. In the LOW position maximum attenuation is inserted. Paragraph 10, below, describes the procedure for obtaining a signal at the desired level.

7. Enable the test signal by placing Bit 0 of Byte 2 in the HIGH position, then pushing the RCVR TEST ENABLE button on the TEST UNIT panel. The lamp on this button should begin to blink.

8. Select desired antenna using the BIT-BOX according to Appendix B.

9. Determine the desired signal amplitude. The nominal test signal is at -93 dBm.

10. Determine the amount of attenuation needed by subtracting the loss tabluated below from the desired signal level. (e.g., if -93 dBm is desired at Antenna 1, the attenuation needed is 93 - 62.2 = 30.8). Round off to nearest .5 dB.

ANTENNA 1	ANTENNA 2	ANTENNA 3
62.2	60.5	61.4

11. Byte 1 of the BIT-BOX sets up required attenuation as follows:

BIT	7	6	5	4	3	2	1	0
dB	32	32	16	8	4	2	1	.5

A switch in the LOW position inserts the corresponding attenuation. The attenuation is added (e.g., Bit 5 LOW plus Bit 4 LOW yields 16 + 8 = 24 dB). Program the switches until the attenuation found in paragraph 10 is established.

12. Turn the signal on and off with Bit 1 of Byte 2. When the switch is on the RCVR TEST lamp is blinking and the antenna lamp corresponding to the selected antenna is on. When the switch is in the HIGH position the Receiver Test signal is activated.

B. TESTING

Push the RECEIVED RF or SSA IF pushbutton corresponding to the antenna in which the test signal is being injected. Tune the Tektronix spectrum analyzes to the frequency of the test signal and observe the signal on the display. A -95 dBm test signal will appear at -45 dBm on the display with the attenuator knob on the TEST UNIT panel set to 0 dBm. With the test signal present, vary its frequency, amplitude and modulation and observe these changes on the spectrum analyzer. If a signal is present but does not correspond to selected frequency, modulation or power, proceed to paragraph 3.

1. If the test signal is not present on the spectrum analyzer, proceed as follows. Replace TEST BOARD II and repeat the procedure above. TEST BOARD II contains the control circuiting for the selection and routing of Receiver Test

signals. If this does not produce results, continue. Connect a cable from the RF IN jack of the Tektronix spectrum analyzer to TR J21 and set up a test signal as if for Antenna 1. Repeat for TR J22 (Antenna 2) and TR J23 (Antenna 3). If the test signal appears, proceed to paragraph 2. If the test signal does not appear in all three cases a problem exists on either TR or TEST BOARD II. If this is the case, check all cables between TU and TR to see that they are connected. Appendix A contains a diagram of all TEST UNIT cable connections. If all cables are in place, replace TEST BOARD II with a new board and repeat the previous tests. If the test signal is still not present, replace the TEST UNIT RF panel (TR).

If these procedures still fail to produce a test signal at the spectrum analyzer, return all cables to their original connections. Locate the panel at the rear of Rack 5 that is labeled ANT 1, ANT2 and ANT 3. With a signal generator, insert a -10 dBm signal of desired frequency into the desired BNC connector. Select the appropriate pushbutton on the TEST UNIT panel and tune the spectrum analyzer to the signal frequency. If the signal appears, the remainder of the system is functioning properly. This method may be used to provide test signals in the absence of a functional Receiver Test section. If the signal still is not present, follow the procedures discussed in paragraph 2.

2. If a test signal is being generated at TR, but does not appear on the spectrum analyzer, one of three conditions can exist; 1, the Spectrum Analyzer section of the TEST UNIT has malfunctioned; 2, the signal is not getting from TR to the RF preamplifier in the antenna deck box; 3, the signal is not getting from the RF preamplifier to the SSA's RF UNIT and SIGNAL SELECTOR.

a. Condition 1 is checked as follows. Set up a test signal for Antenna 1. Disconnect the cable at TR J17. Connect this cable, with an extension, to the RF IN jack on the Tektronix spectrum analyzer. Tune the spectrum analyzer to the frequency of the test signal. If the signal appears on the display, the spectrum Analyzer section of the TEST UNIT has failed. Proceed to Section II of this appendix.

b. Condition 2 is checked by verifying that all cables between the TEST UNIT, the STATION INTERFACE and the antenna deck box are properly installed.

c. Having checked Conditions 1 and 2, the SSA RF UNIT and/or SIGNAL SELECTOR is suspected of failure. Refer to appropriate documentation.

3. If test signals are being generated but are not of the correct power level, frequency or modulation, proceed as follows.

a. Power

Refer to Section IV and verify that the LOW POWER LEVELER is properly calibrated. If so, ensure that the SSA

Frequency Generator is providing a 150 MHz, +20 dBm signal at TR J24, and that L. O. 8 is providing a +13 dBm of correct frequency at TR J20.

b. Frequency

Ensure that the SSA Frequency Generator is providing a 150 MHz, +27 dBm signal to TR J24. Refer to appropriate documentation and ensure that L. O. 8 is being properly programmed by CBL-8.

c. Modulation

If PSK data rates are not correct, replace TEST BOARD I. If still not correct, replace CBL-12. If these steps do not produce desired results, the problem likely lies with the PSK modulator or one of the assemblies on TR. AS a back-up to internally generated PSK data, CBL-12 may be used to select data from the HP1645A Data Error Analyzer (BE). If this is done, BE must be manually set up as to clock rate and length. Refer to the operation manual for the HP1645A for instructions.

II. SPECTRUM ANALYZER SECTION

A. SIGNAL SELECTION

1. Turn the Tektronix 7613/7L12 spectrum analyzer on. Set resolution to 300 kHz, frequency span per division to 1 MHz, and time per division to "Spectrum". Set attenuation to 0 dB (fully CCW).

2. Generate a Receiver Test signal at Antenna 1 at 260 MHz, -95 dBm via the SSA Touch Panel, or inject a 260 MHz, -18 dBm signal at the input to the "ANT 1" jack at the rear of Rack 5.

3. Push the "Received RF, ANT" pushbutton on the TEST UNIT panel. Tune the spectrum analyzer to 260 MHz. There should appear a -55 dBm signal at 260 MHz.

4. Push the "SSA IF, ANT1" pushbutton on the TEST UNIT panel. Tune the spectrum analyzer to 80 MHz. There should appear a -60 dBm signal at 80 MHz.

5. Repeat the precedures listed in paragraphs three and four for Antennas 2 and 3.

6. If a signal does not appear on the spectrum analyzer as described above, locate the jack in Table II.1 corresponding to the missing signal. Inject a signal of known amplitude and frequency directly into this jack. Select the correspondin pushbutton on the TEST UNIT panel. Attempt to locate the signa on the spectrum analyzer. If the signal cannot be located on

TABLE II.1

SELECTED SIGNAL	INPUT JACK
SSA IF ANT 1	TR J10
SSA IF ANT 2	TR J11
SSA IF ANT 3	TR J12
RECEIVED RF ANT 1	TR J17
RECEIVED RF ANT 2	TR J18
RECEIVED RF ANT 3	TR J19
TRANSMITTED RF ANT 1	TR J14
TRANSMITTED RF ANT 2	TR J15
TRANSMITTED RF ANT 3	TR J16

the spectrum analyzer, ensure that all cables between TR and TU are connected. See Figure A.7, Appendix A for a cable diagram. If this signal still does not appear on the spectrum analyzer a fault on the TR panel is suspected. If the signal does appear on the spectrum analyzer the failure exists external to the TEST UNIT.

B. OVERLOAD INDICATOR

Set the attenuation knob on the TEST UNIT panel to 0 dB. Locate the HP33330B detector and the 2" x 2" aluminum box containing the overload circuit. Inject a -10 dBm signal at the input (SMA-MALE) connector of the HP33330B. The overload indicator (LED) on the TEST UNIT panel should be flickering on and off. Increase the power into the detector to 0 dBm. The overload indicator should be on. Turn the attenuation knob on the TEST UNIT panel. The overload indicator should turn off.

C. MARKER FREQUENCY

1. Locate the set of six thumbwheels on the TEST UNIT panel. Adjust the thumbwheels to 70.000 MHz. Tune the spectrum analyzer to 70 MHz. Select the "Marker On" push-button. A robust signal at 70 MHz should appear.

2. Adjust the remaining four thumbwheels through each of its ten positions in turn (i.e., 0 through 9), the marker should shift by the corresponding amount on the display.

3. Adjust the thumbwheels to 250 MHz and repeat the procedures in paragraphs 1 and 2.

4. If the marker does not appear as discussed above, check first to see if the SM-160 is generating the correct frequencies. Do this by disconnecting the cable at TU J14 and the short cable at the RF input to the spectrum analyzer. Connect a cable between TU J14 and RF IN on the spectrum analyzer. Select the "Marker ON" pushbutton. Tune the spectrum analyzer to the IF passband (60 - 90 MHz) and adjust the thumbwheels within this same range. Frequencies observed on the spectrum analyzer should match thumbwheel settings. If the appropriate signals appear, reconnect cables to their original position and proceed to paragraph 5. If the signals do not appear, remove TEST BOARD I and replace it with a new board. If the signals still do not appear, remove the Syntest SM-160 and replace it with a new one. Replace all cables to their original position. Proceed to paragraph 5 if the above procedures have not located the fault.

5. Verify that the SSA Frequency Generator is providing a 1 MHz TTL reference to TR J26 and a 180 MHz, +20 dBm signal to TR J25. Ensure that all cables between TR and TU are connected. See Figure A.7, Appendix A, for a diagram of the cables. If the marker frequency still does not operate, a failure on the TR panel is suspected.

D. TIME-DOMAIN DISPLAY

This section is easily tested by inserting an audio frequency signal at the SSA AUDIO SELECTOR at the jacks corresponding to

each of the five SSA receivers. (SPECTRUM RECEIVERS 1 - 4 and AN/WSC-3). Select VERT MODE and TRIG SOURCE "LEFT" on the Tektronix 7613 mainframe in the TEST UNIT. On the 7A18 dual-trace amplifier, select CH 1. Adjust the thumbwheel to the left of the 7A18 to the receiver position (1 through 5) corresponding to the signal inserted at the AUDIO SELECTOR. The signal should appear on the Tektronix oscilloscope. If the signal does not appear, check the cable from ASJ5 to TU J13. Using a logic probe or a voltmeter, verify correct thumbwheel operation by comparing thumbwheel output with Table 2.4. Check the cable between TU1 J9 and GI J5, and the micro-ribbon cables between TU J8/J9 and TR J2/J3. If these procedures do not solve the problem, refer to documentation on AUDIO SELECTOR.

III. OPERATING TEMPERATURE SECTION

Testing of the Operating Temperature section is most easily accomplished by performing the manual Operating Temperature Test. See Section III and Appendix G for instructions. Upon running the test, the operator should observe a Y-factor (discussed in Section III) on the order of 4 to 9 dB. If a Y-factor is not observed on the Tektronix spectrum analyzer, proceed as follows:

A. Ensure that the spectrum analyzer is set up precisely according to the directions displayed on the Touch Panel. (These directions are also listed in Appendix G). Run the automatic Operating Temperature Test. If a reasonable operating temperature is calculated (in the neighborhood of $500^{\circ}K$), a fault in the Spectrum Analyzer Section of the TEST UNIT or in spectrum analyzer set-up is likely.

B. If neither the manual nor automatic test works, locate WP J10 on the WSC-3 panel. Activate the Operating Temperature Test for all three antennas. There should be +28VDC at pins A, B and C of WP J10; verify this with a voltmeter. (Note that the Operating Temperature Test is controlled by the CPU via CBL12. A BIT-BOX may be substituted for CBL12. See appendix B for the bits that control the Operating Temperature Test.)

1. If +28VDC is present as indicated, proceed to paragraph C.

2. If +28VDC is not present at pins A, B and C with all three activated, check first to ensure that the cable between WP J2 and TR J7 is properly connected. Check the fuses shown in Figure A.10, sheet 4, Appendix A to see that they are properly installed and have not blown. A blown fuse indicates a short to ground in the +28VDC line to the noise diode, probably in the antenna deck box. Correct the short and replace the fuse if this is the case. If the cable is properly connected and the fuses are in place, replace CMB-1 on TUI with a new board.

C. If +28VDC is present at pins A, B and C of WP J10, check all cables between the SSA Station Interface and the antenna deck boxes. Ensure that the cable between WP J10 and SI J3, J9 and J14 is properly connected. Check the installation of the noise diode in the antenna deck box. If the test for one antenna has failed but the others are working, swap two of the noise diodes. If the previously faulty test now performs properly, the orignial noise diode was faulty. REPLACE THE NOISE DIODES IN THEIR ORIGINAL LOCATIONS. Failure to do so will result in uncalibrated results in future tests. If these procedures do not solve the failure, a problem may exist between the RF preamplifier in the antenna deck box and the SSA RF UNITS and/or SIGNAL SELECTOR. Consult appropriate documentation to check these assemblies.

IV. AN/WSC-3 SECTION

A. AN/WSC-3 TRANSMIT

The simplest level test for transmit functions is provided by the SSA software; one of the AN/WSC-3 menus available to the operator sets up a set of parameters (frequency, power, modulation) and transmits the resulting signal into a dummy load at the push of a button. The operator observes the AN/WSC-3 power meter to verify that an RF signal is indeed being transmitted. Presence of power at the dummy load indicates that the basic elements in the software control, the external modem and the AN/WSC-3 itself are functioning.

A more exacting test may be conducted as follows: Replace CBL11 with a BIT-BOX. Refer to Appendix B for CBL11 bit assignments. Enable the transmitter by making byet 2, bit 2 of CBL12 HIGH (this, too, will require a BIT-BOX), then push the XMTR ENABLE pushbutton on the TEST UNIT panel. A local oscillator signal must be provided at WP J7. A signal generator set to 70 MHz at +13 dBm may be used, or L05 (Rockland Synthesizer) may be programmed with a third BIT-BOX. Using the bits of CBL11, set up any desired transmit signal, being sure to select DUMMY LOAD vice any of the antennas. Connect the desired measurement device (power meter, spectrum analyzer) to RS J8, the COUPLE port of the dirctional coupler on RS.

A convenient measurement tool is the TEST UNIT spectrum analyzer; connect a cable from RS J8 to the RF IN port on the 7L12. Either a fixed attenuator must be used or the RF attenuation knob on the Tektronix spectrum analyzer must be used to reduce the signal amplitude into the 7L12; the signal at RS J8 may be as high as +20 dBm. 50 dB of attenuation should be introduced.

Once the transmitter and measurement device are set up, CBL11 may be used to run the AN/WSC-3 through the gamut of operating parameters. Frequency, power level and modulation may all be varied and the resulting changes noted. Byte 2, Bit 3 of CBL12 may be used to key the transmitter on and off, or it may be left on (HIGH).

If no RF power is being transmitted, check first to see that the AN/WSC-3 is properly set up. See Section V.B. If so, turn the FREQUENCY SELECT switch to MANUAL and dial a valid transmit frequency on the AN/WSC-3 thumbwheels. If the signal appears, a fault in the frequency control modification is indicated. If not, return the switch to the PRESET position and turn the REMOTE LOCAL switch to REMOTE. Turn the AN/WSC-3 power meter to mid range. Key the transmitter with CBL-12 byte 2, bit2. Locate the BITE select switch on the AN/WSC-3 and turn it to position 11. Toggle the BITE test switch; the BITE meter should be in the "GOOD" region indicating that the keyline is indeed present. If a transmitted signal appears.

a fault in the High Power Leveler is indicated.

If these procedures fail to produce a signal, slide the AN/WSC-3 partially out of its cabinet and put the modification control toggle switch in the "WSC-3 NORMAL" position. Select MANUAL, LOCAL operation, and EXTERNAL MODEM. Attempt to key the transmitter with the Test Key on the AN/WSC-3 front panel. Select PSK modulation and repeat the last step. If the signal appears when the radio is manually keyed when PSK is selected, but not when EXT MODEM is selected, a problem with the external modem section of WP is likely. If the signal appears in neither case, the AN/WSC-3 has failed.

B. AN/WSC-3 RECEIVE

CW and PSK reception may be tested from the TOUCH PANEL by generating a Receiver Test signal, injecting it into a desired antenna, then routing it to the AN/WSC-3 via the signal selector. Similarly, CBL11 and CBL12 may be replaced with BIT-BOXES and the tests set up manually. AM/FM reception is verified by injecting a test signal directly into the receive antenna jack of the AN/WSC-3. If the system is operating properly, recovered PSK may be monitored at the Data Interface and received AM/FM is present at the AUDIO SELECTOR.

If a known signal, present at the antenna, cannot be recovered by the AN/WSC-3, the first step that must be taken is to isolate the AN/WSC-3 section from the remainder of the SSA RF chain. This is easily accomplished by removing the cable at WP J6. (This is the cable from the Signal Selector.) Next

set up a known signal according to the instructions in Section I of this appendix. Disconnect the cable at the output of TR AT3 and connect a cable from RT J9 to the output of TR AT3. That is, connect the output of the second of the programmable attenuators of the Receiver Test section of TR to the input of the AN/WSC-3. Adjust the attenuation via CBL12 so that the signal at RT J9 is at -66 dBm. Verify that the AN/WSC-3 is operating correctly by selecting LOCAL mode and MANUAL frequency select and tuning the radio to the frequency of the known signal. Select the appropriate demodulation with the modulation switch and attempt to recover the signal at the Data Interface or Audio Selector as appropriate. If the signal is not recovered, the AN/WSC-3 has failed.

When the AN/WSC-3 is known to be properly working, place the radio in the REMOTE/PRESET configuration and attempt to control it via CBL11. Select frequency and modulation mode according to Appendix B, and monitor the Data Interface or Audio Selector. If the signal cannot be recovered, a problem with the CBL11 interface at the Test Transmitter board may exist. No electronic parts are involved; check WP J13, WP J17 and WP J19 against the wire list in Appendix E and the schematic of WP in Appendix A.

The RF hardware on WP may now be checked by applying a 90 MHz, +13 dBm signal at WP J7 from a signal generator. Apply on 80 MHz, -66 dBm 10% AM signal at WP J5. Use CBL11 to tune the AN/WSC-3 to 260 MHz and to select the AM demodula-

tion mode. The demodulated audio signal should be present at the Audio Selector. If not, connect the output of the receive section of WP (WP J15) to a spectrum analyzer, such as the Tektronix 7L12 in the TEST UNIT, to verify the presense of a signal.

APPENDIX D

PARTS LIST

Title TEST UNIT, Front Panel (TU) Drawing TU

	Reference Designation	Description
1	A1	Tektronix 7L13/7L12/7A18
2	A2	Syntest SM160 Frequency Synth.
3	A3	Test Board 1
4	A4	Test Board 2
5	AT1	Telonic 8121S Step Attenuator
6	R1	10Ω , 10W Resistor
7	D1	Jan 1N485B Diode
8	D2	Jan 1N485B Diode
9	D3	Jan 1N485B Diode
10	J1-J4	Ansley 609-5005 PC Edge Connector
11	J5	TRW Cinch 50-44A-30 Edge Conn.
12	J6, J7, J9	Ansley 609-50F Ribbon Connector
13	8	Amphenol 57-40500 Ribbon Connector
14	J10, J13	King UG-492 D/U BNC Feedthru
15	LAMP 1-21	Dialite 554-1001-211 Indicator Lamp
16	S1-S20	Dialite 554-3121-211 Spdt Momentary SW
17	S21	Dialite 554-1121-211 Spdt Mom. Switch

18	S15	Cherry T-75-04-M Thumbwheel Switch (X1)
19	S16	Cherry T-75-04-M Thumbwheel Switch (6)
20	TM 1	FT-50 Feedthru Termination ELCOM
21	LED1	LED, 5VDC, DIALCO 249-7868
22	LED2	LED, 5VDC, DIALCO 249-7868

Title Test Board 1 Drawing TU

	Reference Designation	Description
1	U1	19.2 KC Oscillator
2	U2-U6	7474 Dual D Flip-Flop
3	U7	74164 Serial in Parallel Out Shift Register
4	U8	74260 Dual 5 - Input NOR Gate
5	U9	74151 8 Line Multiplexor
6	U10	7404 Hex Inverter
7	U11	7486 Quad 2-Input XOR Gate Quad
8	U12	7403 Quad 2-Input NAND w/Open Collector Outputs
9	U13	7400 Quad 2-Input NAND Gate
10	U14	7408 Quad 2-Input and Gate
11	U15	7427 Triple 3-Input NOR Gate
12	U16	LM555 Timer
13	U17	7404 HEX Inverter
14	U18	7400 Quad 2-Input NAND
15	U19	LM7810 +10VDC Voltage Regulator
16	U20	LM340-24 +24 VDC Voltage Regulator
17	U21	ULN2003A Driver
18	U22	74186 64 x 8 Fuzeable Link Prom
19	U23	7404 HEX Inverter

20	U24	316A322 2.2KΩ DIP Resistor Pack
21	U25	314A322 2.2KΩ DIP Resistor Pack
22	U26	316A322 2.2KΩ DIP Resistor Pack
23	C1	10 mf Tantalum Capacitor
24	C2,C3	1 mf Tantalum Capacitor
25	C4,C5	2.2 mf Tantalum Capacitor
26	C6-C28	.1 mf DIP Despiking Capacitor
27	R1,R2	10Ω 10W Resistor
28	R3	5Ω 10W Resistor
29	R4	4Ω 10W Resistor
30	R5,R6,R12	5Ω 10W Resistor
31	R7	5.6KΩ 1/4W Resistor
32	R8,R9,R13-R24	1KΩ 1/4W Resistor
33	R10	3KΩ 1/4W Resistor
34	R11	100KΩ 1/4W Resistor
35	D1	Light Emitting Diode

Title Test Board II Drawing TU

	Reference Designation	Description
1	U1	74148 8 Bit Priority Encoder
2	U2	7400 Quad 2 Input Nand Gate
3	U3	74175 Quad D Flip-Flop
4	U4	314A22 Resistor
5	U5	74H22 Dual 4 Input Nand
6	U6	7422 BCD to Decimal Decoder
7	U7, U8	7404 Hex Inverter
8	U9, U10	ULN2003 Driver
9	U11	7408 Quad 2 Input and Gate
10	U12	7474 Dual D Flip-Flop
11	U13	7404 Hex Inverter
12	U14	7408 Quad 2 Input and Gate
13	U15	7474 Dual D Flip-Flop
14	U16	ULN2003 Driver
15	U17	7404 Hex Inverter
16	U18	7408 Quad 2 Input and Gate
17	C1-C9	.001 mf Capacitor
18	C14, C24, C25	.047 mf Capacitor
19	C10-C13, C15-C23	.1 mf Dip Capacitor
20	R1-R4	1kΩ, 1/4 Watt Resistor
21	R5, R6	5.6KΩ, 1/4 Watt Resistor

Title Test Unit RF Panel (TR) Drawing TR

	Reference Designation	Description
1	AMPL1	Amplifier, WJ6200-352
2	AMPL2	Amplifier, QB 512
3	AMPL3	Amplifier, QB 512
4	AMPL4	Amplifier, QB 512
5	A1	Overload Circuit
6	AMPL5	Amplifier, QB 300
7	A2	Low Power Leveler
8	AT1	Attenuator, AT-50-6
9	AT2	Attenuator, 100D 0589-A-8-16-32-32
10	AT3	Attenuator, 100D 0589-A-4-A-12
11	AT4	Attenuator, AT-50-10
12	AT5	Attenuator, AT-50-3
13	AT6	Attenuator, AT-50-3
14	CP1	Coupler, ZFDC-10-1
15	CP2	Coupler, ZFDC-20-3
16	CP3	Coupler, ZFDC-10-1
17	PD1	Splitter, PDM-20-250
18	MX3	Mixer, Merrimac, DMM 4-250
19	AT7	Variable Attenuator, Merrimac, ARM-1
20	AT8	Variable Attenuator, Merrimac, ARM-1
21	AT9	Variable Attenuator, Merrimac, ARM-1
22	AT10	Variable Attenuator, Merrimac, ARM-1
23	AT11	Variable Attenuator, Merrimac, ARM-1
24	AT12	Variable Attenuator, Merrimac, ARM-1

Title Test Unit RF Panel (TR) Drawing TR

	Reference Designation	Description
25	DET1	Detector, HP33330B-003
26	DET2	Detector, HP33330B-003
27	MOD1	PSK Modulator, P4-BPM-90TTL
28	MX1	Mixer, CM-1
29	MX2	Mixer, DMM-4-250
30	FL1	Low Pass Fltr, 4420,156/10-0
31	FL2	Band Pass Fltr, 3B120-180/10-0
32	FL3	Notch Fltr, 4N30-180/3.5-0
33	FL4	Band Pass Fltr, 4B120-257/40-0
34	S1	Electronic Switch, Lorch, ES391M
35	S2	Electronic Switch, Lorch, ES387M
36	S3	Electronic Switch, Lorch, ES391M
37	S4	Electronic Switch, Lorch, ES393M
38	S5	Electronic Switch, Lorch, ES387M
39	J1	Plug, 14 Pin, MS3106A 22-19S
40	J29	Plug, 37 Pin, DC-37P
41	M1	Box, Aluminum, 2" x 2" x 1.5"
42	M2	Box, Aluminum, 2" x 5" x 1.5"

Title Overload Circuit Drawing TR

	Reference Designation	Description
1	U1	NE527 Comparator
2	U2	7812 + 12VDC Voltage Regulator
3	U3	7912 -12VDC Voltage Regulator
4	R1,R2	4.7kΩ 1/4W Resistor
5	R3	18kΩ 1/4W Resistor
6	R4	200Ω 12 Turn Trim Pot
7	C1,C2	1mf Tantalum Capacitor
8	C3,C4	2.2 mf Tantalum Capacitor

Title Low Power Leveler Drawing TR

	Reference Designation	Description
1	R1	3.3kΩ 1/4W Resistor
2	R2-R4	10kΩ 1/4W Resistor
3	R5	470Ω 1/4W Resistor
4	R6	200Ω 12 Turn Trim Pot
5	C1	220 pf Capacitor
6	C2,C5	1mf Tantalum Capacitor
7	C3,C4	2.2mf Tantalum Capacitor
8	D1	Jan IN 485 B Diode
9	E1	Electronic Attenuator, Microcircuits, PAS-1
10	U1	LM741 Operational Amplifier
11	U2	7812 +12VDC Voltage Regulator
12	U3	7912 -12VDC Voltage Regulator

Title Control Motherboard 1 Drawing TUI

	Reference Designation	Description
1	U1	7404 Hex Inverter
2	U2	7408 Quad 2-Input and Gate
3	U3	7432 Quad 2-Input or Gate
4	U4	9602 Dual, Retriggerable One-Shot Multivibrator
5	U5	LM555 Timer
6	U6	7400 Quad 2-Input Nand Gate
7	K1,K2,K3	PRMA 1A05C Dip Relay
8	R1-R8	1kΩ 1/4W Resistor
9	R9,R10	18kΩ 1/4W Resistor
10	R11	2MΩ 1/4W Resistor
11	R12	3.3kΩ 1/4W Resistor
12	R13	50kΩ 1/4W Resistor
13	C1	100 mf 25WVDC Electrolitic Capacitor
14	C2	1 mf Capacitor
15	Q1,Q2	2N3704 NPN Transistor
16	J26	Amphenol 2058-0000 SMA Female Connector
17	C3-C7	.1 mf Despiking Capacitor

Title WSC-3 Panel (WP) Drawing WP

	Reference Designation	Description
1	CP1	10 dB Coupler, ZFDC-10-1
2	DBL1	Freq. Doubler, D1-4
3	FL1	Band Pass Fltr, 3050-70/5-0
4	FL2	Band Pass Fltr, 3B120-180/10-0
5	FL3	Band Pass Fltr, 3B50-70/5-0
6	MOD1	PSK Modulator, P4-BPM-90TTL
7	MX1	Mixer, DMM 4-250
8	DET1	Detector, HP3330B-003
9	CP2	30dB Coupler, Narda, 3000-30
10	AMPL1	Amplifier, Anzac, AM 105
11	AMPL2	Amplifier, Anzac, AM 102
12	AMPL3	Amplifier, Anzac, AM 102
13	AT1	Attenuator, Elcom, AT-50-5
14	AT2	Attenuator, Elcom, AT-50-3
15	AT3	Attenuator, Elcom, 100C-1427-2
16	J18	Edge Connector, CINH, 225-21821-401-117
17	J19	Edge Connector, CINCH, 6AD01-25-1A1-00
18	S1	Switch, Momentary, ALCO, MSP105F
19	J1	Socket, 14 Pin, AMPHENOL, MS3106 21-195
20	J4	Socket, 3 Pin, AMPHENOL, MS3102A 14S-3S
21	J5	Plug, 25 Pin, ANSLEY, 609-25P
22	J10	Socket, 4 Pin, AMPHENOL, MS3102R 14S-4S
23	J12	Socket, 36 Pin, AMPHENOL, 57-40360

Title WSC-3 Panel (WP) Drawing WP

	Reference Designation	Description
24	J13	Socket, 24 Pin, AMPHENOL, 57-40240
25	J17	Socket, 50 Pin, AMPHENOL, 57-40500
26	A4	PC Board Test Transmitter Bd
27	A5	PC Board Control Motherboard II
28	J20	Socket, 2 Pin, MS3107A 12S-2S
29	K1	Relay, Potter and Brumfield, KRP11DG
30	D1,D2,D3	Jan W485B Diode
31	F1	Fuse, 1 Amp
32	F2	Fuse, 1 Amp
33	F3	Fuse, 1 Amp
34	R1	68Ω, 1W Resistor
35	R2	2.2kΩ, $\frac{1}{4}$W Resistor
36	R3	2.2kΩ, $\frac{1}{4}$W Resistor
37	R4	2.2kΩ, $\frac{1}{4}$W Resistor

Title Test Xmtr Board Drawing WP-C-14

	Reference Designation	Description
1	U1	74260 Dual 5-input Nor Gate
2	U2	74164 Serial in Parallel Out Shift Register
3	U4-U7	7474 Dual D Flipflop
4	U8	19.2KC Oscillator
5	U9	7403 Quad 2-Input Nand Gate w/ open Collector Outputs
6	U10	7486 Quad 2-Input XOR Gate
7	U11	7404 Hex Inverter
8	U12	74151 8 Line Multiplexor
9	U13,U14	LM741 Operational Amplifier
10	U15	LM 318 Operational Amplifier
11	U16	7408 Quad 2-Input and Gate
12	U17,U23	7432 Quad 2-Input or Gate
13	U18,U19	ULN2003A Driver
14	U20	7404 Hex Inverter
15	U21	7812 +12 vdc Voltage Regulator
16	U22	7912 -12 vdc Voltage Regulator
17	R1-R3	1kΩ 1/4 W Resistor
18	R4,R7,R9	18kΩ 1/4 W Resistor
19	R5,R6,R14,R10,R11	10kΩ 1/4 W Resistor
20	R8,R17	3.3kΩ 1/4 W Resistor
21	R12,R13	20kΩ 1/4 W Resistor
22	R15	1kΩ 10 Turn Trim Pot

Title Test Xmtr Board Drawing WP-C-14

	Reference Designation	Description
23	R16	1mΩ 10 Turn Trim Pot
24	C1,C4	1mf Tantalum Capacitor
25	C2,C3	2.2mf Tantalum Capacitor
26	C5,C9-C13	.1mf Dip Despiking Capacitor
27	C6,C7	47 pf Capacitor
28	C8	.1mf Capacitor
29	D1	755A 7.5V Zener Diode
30	D2-D4	IN4148 Diode
31	C14-C17	100 pf Capacitor

Title Control Motherboard II Drawing WP

	Reference Designation	Description
1	U1,U2	8T16 RS232 to TTL Converter
2	U3	8T15 TTL to RS232 Converter
3	CL,C3	1 mf Tantalum Capacitor
4	C2,C4	2.2 mf Tantalum Capacitor
5	VR1	+12BDC Pos. 12 Volt Regulator
6	VR2	-12VDC Neg. 12 Volt Regulator

Title Data Interface Panel (D1) Drawing ____

	Reference Designation	Description
1	J1	Plug, 15 Pin DA15P
2	J2	BNC Feedthru UG-492D/U
3	J3	BNC Feedthru UG-492D/U
4	J4	BNC Feedthru UG-492D/U
5	J5	BNC Feedthru UG-492D/U
6	J6	BNC Feedthru UG-492D/U
7	S1	Switch, Toggle MST105D

Title RF Switching Panel (RS) Drawing ____

	Reference Designation	Description
1	S1	Transfer Swtich, Teledyne CS-37
2	S2	Transfer Switch, Teledyne CS-37
3	S3	Transfer Switch, Teledyne CS-37
4	S4	Transfer Switch, Teledyne CS-37
5	S5	Transfer Switch, Teledyne CS-37
6	TM-1	Coaxial Load Bird 8160
7	TM-2	Coaxial Load Bird 8071
8	TM-3	Coaxial Load Bird 8071
9	TM-4	Coaxial Load Bird 8071
10	TM-5	Coaxial Load Bird 8071
11	TM-6	Coaxial Load Bird 8071
12	TM-7	50Ω Termination, Ellom, CT-50
13	CP1	Directional Coupler, Narda, 3040-30

APPENDIX E

WIRE LIST

WPJ2	TRJ7	Purpose
1	1	Ground
2	2	HP1645A Data to Rcvr Test
3	3	NC
4	4	NC
5	5	NC
6	6	NC
7	7	NC
8	8	RS S-5
9	9	Rcvr Test Monitor
10	10	RS S-4
11	11	RF Keyline
12	12	RS S-3
13	13	Noise Temperature Test 1
14	14	RS S-2
15	15	Noise Temperature Test 2
16	16	RS S-1
17	17	Noise temperature Test 3
18	18	+28VDC
19	19	Remote/Local Status
20	20	NC
21	21	Operate/Standby Status

WPJ2	TRJ7	Purpose
22	22	NC
23	23	XMTR RF Above 1 Watt Status
24	24	NC

WPJ3	BE DATA INTERFACE	Purpose
2	14	NC
4	15	NC
6	16	NC
8	17	NC
10	18	NC
12	19	NC
14	20	NC
16	21	NC
18	22	HP1645 Clock Out
20	23	NC
22	24	NC
24	25	NC
1	1	Chassis Ground
3	2	Data From HP1645A
5	3	Data to HP1645A
7	4	NC
9	5	NC
11	6	NC
13	7	Signal Ground
15	8	NC
17	9	NC
19	10	NC
21	11	NC
23	12	NC
25	13	NC

WPJ5	RSJ1	Purpose
1	1	+28
2	2	+28 Return
3	3	RS-S1 Relay
4	4	RS-S2 Relay
5	5	RS-S3 Relay
6	6	RS-S4/S5 Relay
7	7	Status Return
8	8	RS-S1 Status
9	9	RS-S2 Status
10	10	RS-S3 Status
11	11	RS-S4 Status
12	12	RS-S5 Status

WPJ11	DIJ1	Purpose
1	1	NC
2	9	Ground
3	2	NC
4	10	NC
5	3	NC
6	11	WSC-3 Bit Timing Out
7	4	NC
8	12	WSC-3 PSK Data Out
9	5	WSC-3/External Select; Common Term.
10	13	NC
11	6	WSC-3/External Switch; WSC-3 Term.
12	14	Test XMTR Monitor
13	7	WSC-3/External Switch; External Term.
14	15	RCVR Test Monitor
15	8	TTL IN
16	-	NC

WPJ12	RTJ2	Purpose
4	18	XMTR RF ABove 1 Watt
5	36	WB/NB
6	38	Operate/Standby Status
7	33	RF Keyline
8	42	PSK Data In
9	43	PSK Return
10	44	PSK Shield
11	67	PSK Data Out
12	68	PSK Return
13	69	PSK Shield
14	70	Clock In
15	71	Clock Return
16	76	Clock Out
17	77	Clock Return
18	79	Chassis Ground
19	48	Keyline Interlock (Jumper)
20	49	Keyline Interlock (Jumper)

WPJ13	RTJ3	Purpose
1	H	Modulation Code A
2	J	Modulation Code B
3	K	Modulation Code C
4	L	Modulation Code D
5	M	Modulation Code Return
6	V	Ground
7	i	Remote/Local Status
8	j	Remote/Local Return
13	m	Audio
15	n	Audio Return
14	p	Shield

WPJ17	Purpose
1	200/300 MHz
2	10 MHz 8
3	10 MHz 4
4	10 MHz 2
5	10 MHz 1
6	1 MHz 8
7	1 MHz 4
8	1 MHz 2
9	1 MHz 1
10	100 kHz 8
11	100 kHz 4
12	100 kHz 2
13	100 kHz 1
14	25 kHz 02
15	25 kHz 03
16	Return
17	Leveler reference
18	Leveler output
19	NC
20	NC
21	NC

WPJ18 is bottom of Control Motherboard 2 CMB-2)

WPJ18	Purpose	Destination
D	Xmtr RF Above 1 W	WPJ4 Pin 4
E	OP/Stdby	WPJ4 Pin 6
F	Remote/Local	WPJ13 Pin 7
H	NF3	WPJ2 Pin 17
J	NF2	WPJ2 Pin 15
K	NF1	WPJ2 Pin 13
L	RF Keyline	WPJ12 Pin 7
M	+5	
N	+5 Return	
P	NC	
R	NC	
T	NC	
U	NC	
V	Test Xmtr Monitor	WPJ19 Pin 8
1	+28	
2	(Status) RS S1	WPJ5 Pin 8
3	(Status) RS S2	WPJ5 Pin 9
4	(Status) RS S3	WPJ5 Pin 10
5	(Status) RS S4	WPJ5 Pin 11
6	(Status) RS S5	WPJ5 Pin 12
7	HP1645 Data	WPJ19 Pin 7
8	PSK Data to WSC-3	WPJ12 Pin 8
9	PSK Data Return	WPJ12 Pin 9
10	Clock in to WSC-3	WPJ12 Pin 14

WPJ18	Purpose	Destination
11	WSC-3 PSK Out Return	WPJ12 Pin 12
12	WSC-3 PSK Out	WPJ12 Pin 11
13	WSC-3 Bit Timing Out	WPJ12 Pin 16
14	WSC-3 Bit Timing Return	WPJ12 Pin 15
15	WSC-3 Bit Timing Return	WPJ12 Pin 17
16	+15	
17	GND	
18	-15	

WPJ19 is Connector at Bottom of Test Xmtr Board

WPJ19	Purpose	Destination
A1	+5	
A2	+5 Return	
A3	Leveler Output	WPJ17 Pin 18
A4	Reference to Leveler	WPJ17 Pin 17
A5	Leveler Input	HP33330B
A6	Data to PSK Modulator	
A7	HP1645 Input	WPJ18 Pin 7
A8	Test Xmtr Monitor	WPJ11 Pin 12
A9	Freq Sel 10 MHz (4)	WPJ17 Pin 3
A10	Freq Sel 10 MHz (1)	WPJ17 Pin 5
A11	Freq Sel 10 MHz (8)	WPJ17 Pin 2
A12	Freq Sel 10 MHa (2)	WPJ17 Pin 4
A13	Freq Sel 1 MHz (4)	WPJ17 Pin 7
A14	Freq Sel 1 MHz (1)	WPJ17 Pin 9
A15	Freq Sel 1 MHz (8)	WPJ17 Pin 6
A16	Freq Sel 1 MHz (2)	WPJ17 Pin 8
A17	Freq Sel 100 kHz (4)	WPJ17 Pin 11
A18	Freq Sel 100 kHz (1)	WPJ17 Pin 13
A19	Freq Sel 100 kHz (8)	WPJ17 Pin 10
A20	Freq Sel 100 kHz (2)	WPJ17 Pin 12
A21	25 kHz D2	WPJ17 Pin 14
A22	25 kHz D3	WPJ17 Pin 15
A23	200/300 MHz Sel	WPJ17 Pin 1
A24	Return	WPJ17 Pin 16
A25	Return	

TRJ9 (STATUS)	CISJ5	Purpose
1	1	XMTR RF Above 1 Watt
2	13	RF Keyline Status
3	2	WSC-3 Remote/Local
4	14	RCVR Test On
5	3	WSC-3 Operate/Standby
6	15	Hi Power Leveler Fault
7	4	RF Switch S-7
8	16	RF Switch S-8
9	5	RF Switch S-9
10	17	RF Switch S-10
11	6	RF Switch S-11
12	18	Low Power Leveler Fault
13	7	RCVR Output Select $\overline{1}$
14	19	RCVR Output Select $\overline{2}$
15	8	RCVR Output Select $\overline{4}$
16	20	Return

For TRJ7 see WPJ2

TRJ2	TUJ8	Purpose
1	1	+5 VDC
2	26	+5 VDC
3	2	Return
4	27	Return
5	3	Byte 3, Bit 4 Clock Select B1
6	28	HP1645/Internal Data Select
7	4	Byte 3, Bit 4 Clock Select B0
8	29	HP1645A Data In
9	5	MLS to PSK Modulator & Monitor
10	30	Overload Indicator
11	6	S2 "1" (Select 60-90 for Marker)
12	31	NC
13	7	S2 "2" Select 240-320 Marker
14	32	+28
15	8	CW/PSK Select
16	33	+28
17	9	Byte 3, Bit 6 Clock Select B2
18	34	+28
19	10	+28V
20	35	+28V
21	11	+28V
22	36	Return
23	12	Return
24	31	Return
25	13	Return

TRJ2	TUJ8	Purpose
26	38	Blink
27	14	NC
28	39	Ground
29	15	1 MHz Ref to SM160
30	40	Ground
31	16	NC
32	41	NC
33	17	NC
34	42	NC

TUJ8	Purpose	Destination
1	+5VDC	J6/1 & J7/1
2	Return	J6/2 & J7/2
3	PSK Clock Select B1	J6/5
4	PSK Clock Select B0	J6/30
5	Data to PSK Moudlator	J6/4
6	TR S2-1	J6/7
7	TR S2-2	J6/32
8	CW/PSK Select	J6/3
9	PSK Clock Select B2	J6/29
10	+28 VDC	NC
11	+28 VDC	J6/37
12	Return	J6/12 & Lamp Test N.O.
13	Return	NC
14	NC	NC
15	Reference to SM-160	J5/K
16	RCVR Select	Receiver Thumbwheel 4
17	RCVR Select	Receiver Thumbwheel 1
18	NC	NC
19	NC	NC
20	NC	NC
21	NC	NC
22	NC	NC
23	NC	NC
24	NC	NC
25	NC	NC

TUJ8	Purpose	Destination
26	+5VDC	J6/26 & J7/26
27	Return	J6/27 & J7/27
28	BE/Internal Data Select	J6/28
29	BE Data In	J6/38
30	Overload Indicator	Overload LED 2
31	NC	NC
32	+28VDC	NC
33	+28VDC	NC
34	+28VDC	NC
35	+28VDC	J6/36
36	Return	NC
37	Return	J2/1
38	Blink	J5/1
39	Return	J5/A
40	RCVR Select	Receiver Thumbwheel 2
41	NC	NC
42	NC	NC
43	NC	NC
44	NC	NC
45	NC	NC
46	NC	NC
47	NC	NC
48	NC	NC
49	NC	NC
50	NC	NC

NOTE: Need +5 volts to + terminal on "Freq invalid" & "overload" led's.

TUJ6	DESTINATION
1	J8 Pin 1
2	J3 Pin 2
3	J8/8
4	J8/5
5	J8/3
6	Marker Off Switch
7	J8/6
8	Lamp Test Switch
9	Lamp Test Switch
10	Marker Off Lamp
11	Freq Invalid
12	J8/12
13	J8/35
14	TW1 - $\overline{1}$
15	TW1 - $\overline{4}$
16	TW2 - $\overline{1}$
17	TW2 - $\overline{4}$
18	TW3 - $\overline{1}$
19	TW3 - $\overline{4}$
20	TW4 - $\overline{1}$
21	TW4 - $\overline{4}$
22	TW5 - $\overline{1}$

TUJ6	DESTINATION
23	TW5 - $\overline{4}$
24	TW6 - $\overline{1}$
25	TW6 - $\overline{4}$
26	J8/26
27	J8/27
28	J8/28
29	J8/9
30	J8/4
31	Marker On Switch
32	J8/7
33	Lamp Test Switch
34	Lamp Test Switch
35	Marker On Lamp
36	J8/36
37	J8/11
38	J8/29
39	TWL - $\overline{2}$
40	TW1 - $\overline{8}$
41	TW2 - $\overline{2}$
42	TW2 - $\overline{8}$
43	TW3 - $\overline{2}$
44	TW3 - $\overline{8}$
45	TW4 - $\overline{2}$
46	TW4 - $\overline{8}$
47	TW5 - $\overline{2}$

TUJ6	DESTINATION
48	TW5 - $\overline{8}$
49	TW6 - $\overline{2}$
50	TW6 - $\overline{8}$

TUJ7	DESTINATION
1	J8/1
2	J8/2
3	X2 Switch N.O.
4	RC2 Switch N.O.
5	X1 Switch N.O.
6	RS2 Switch N.O.
7	Not Conn
8	Not Conn
9	X3 Switch N.O.
10	NC
11	NC
12	NC
13	RC3 Lamp L
14	RC1 Lamp L
15	X1 Lamp L
16	RS2 Lamp L
17	X3 Lamp L
18	RT3 Lamp L
19	NC
20	XMTR Enable Lamp L
21	XMTR Enable Switch N.O.
22	XT3 Lamp L
23	XT2 Lamp L
24	XT1 Lamp L
25	Dummy Load Lamp L

TUJ7	DESTINATION
26	J8/26
27	J8/27
28	RC1 Switch N.O.
29	RC3 Switch N.O.
30	RS3 Switch N.O.
31	RS1 Switch N.O.
32	Not Conn
33	Lamp Test SW. C
34	NC
35	NC
36	NC
37	J8/36
38	RC2 Lamp L
39	x2 Lamp L
40	RS3 Lamp L
41	RS1 Lamp L
42	RT2 Lamp L
43	RT1 Lamp L
44	RCVR Test Lamp L
45	RCVR Test Switch
46	NC
47	NC
48	NC
49	NC
50	NC

RC1,2,3 = RCVR IF XT1,2,3 = TEST XMTR

RS1,2,3 = RCVR RF RT1,2,3 = RCVR TEST

X1,2,3 = XMTR RF

TRJ3	TUJ9	PURPOSE
1	1	NC
2	26	S3 RC3 Control
3	2	S3 RC2 Control
4	27	S3 RC1 Control
5	3	S3 X 2 Control
6	28	34 X 3 Control
7	4	S1 RT3 Control
8	29	S1 RT2 Control
9	5	S1 RT1 Control
10	30	S3-S4 Transition
11	6	S4 RS2 Control
12	31	S4 RS3 Control
13	7	S4 X 1 Control
14	32	S4 RS1 Control
15	8	RT3 Select
16	33	RT2 Select
17	9	RT1 Select
18	34	NC
19	10	NC
20	35	RCVR Enable/Disable

TRJ3	TUJ9	PURPOSE
21	11	RCVR On/Off
22	36	NC
23	12	Test XMTR Enable/Disable
24	37	Test XMTR On/Off
25	13	NC
26	38	NC
27	14	Return
28	39	Return
29	15	Return
30	40	Return
31	16	Return
32	41	Return
33	17	Return
34	42	Return
35	18	Return
36	43	Return
37	19	Return
38	44	XT3 Lamp Contact
39	20	Return
40	45	NC
41	21	NC
42	46	XT2 Lamp Contact
43	22	XT1 Lamp Contact
44	47	Dummy Load Lamp Contact

TRJ3	TUJ9	PURPOSE
45	23	NC
46	48	+28 Return
47	24	NC
48	49	+28
49	25	RF Keyline
50	50	Blink

JACK	CONNECTOR	MATE	FUNCTION	CABLE	CONNECTOR	SOURCE & JACK	CONNECTOR ON SOURCE
Mnemonic: DI							
Assembly Name: Data Interface							
J1	Cinch DA15P	Ansley 609-15S	Interface	Micro-Ribbon	Ansley 609-1615M	WPJ11	16 Pin Edge
Mnemonic: BE							
Assembly Name: HP1645A Bit Error Rate Analyzer							
Data Interface	25 Pin Female Connector	Ansley 609-25P	Interface	Micro-Ribbon	Ansley 609-4015M	WPJ3	40 Pin Edge
Mnemonic: TU							
Assembly Name: Test Unit Front Panel and Drawer							
J8	Amphenol 57-40500	Ansley 609-50M	Control/ Logic	50 Lead Micro-Ribbon	Ansley 609-3415M	TRJ2	34 Pin Edge
J9	Ansley 609-50F	Ansley 609-50M	Control/ Logic	50 Lead Micro-Ribbon	Ansley 609-5015	TRJ3	50 Pin Edge
J10	BNC Female	BNC Male	RF IN	RG223	SMA M	TRJ4	SMA Female
J11	SMA Female	SMA Male	Attenuation	RG223	SMA M	TRJ5	SMA Female
J12	SMA Female	SMA Male	Attenuation	RG223	SMA M	TRJ6	SMA Female

JACK	CONNECTOR	MATE	FUNCTION	CABLE	CONNECTOR	SOURCE & JACK	CONNECTOR ON SOURCE
Mnemonic: TR							
Assembly Name: Test Unit RF Panel							
J1	MS3106A 22-19S	MS3106A 22-19P	DC Power				
J2	34 Pin Edge	Ansley 609-3415M	Control/ Logic	Micro-Ribbon	Ansley 7609-50M	TUJ8	Amphenol
J3	50 Pin Edge	Ansley 609-5015M	Control/ Logic	Micro-Ribbon	Ansley 609-50M	TUJ9	Ansley 609-50F
J4	SMA F	SMA M	RF IN	RG223	BNC M	TUJ10	BNC F
J5	SMA F	SMA M	ATTEN	RG223	SMA M	TUJ11	SMA F
J6	SMA F	SMA M	ATTEN	RG223	SMA M	TUJ12	SMA F
J7	34 Pin Edge	Ansley 609-3415M	Interface	Micro-Ribbon	Ansley 609-3415M	WPJ2	34 Pin Edge
J8	50 Pin Edge	Ansley 609-5015M	CBL-11	Micro-Ribbon	Ansley 609-5015M	CBL-14	50 Pin Edge
J9	16 Pin Edge	Ansley 609-1615M	Status	Micro-Ribbon	Ansley 609-24M	CISJ5	Amphenol 57-40240
J10	SMA F	SMA M	RC1	RG223	SMA M	SSJ8	SMA F
J11	SMA F	SMA M	RC2	RG223	SMA M	SSJ9	SMA F
J12	SMA F	SMA M	RC3	RG223	SMA M	SSJ10	SMA F
J13	SMA F	SMA M	L05	RG223	SMA M	LIJ9	SMA F
J14	SMA F	SMA M	X1	RG223	SMA M	RF1J3	SMA F
J15	SMA F	SMA M	X2	RG223	SMA M	RF2J3	SMA F
J16	SMA F	SMA M	X3	RG223	SMA M	RF3J3	SMA F
J17	SMA F	SMA M	RS1	RG223	SMA M	RF1J5	SMA F
J18	SMA F	SMA M	RS2	RG223	SMA M	RF2J5	SMA F

JACK	CONNECTOR	MATE	FUNCTION	CABLE	CONNECTOR	SOURCE & JACK	CONNECTOR ON SOURCE
Mnemonic: TR [CONTINUED]							
Assembly Name: Test Unit RF Panel							
J19	SMA F	SMA M	RS3	RG223	SMA M	RF3J5	SMA F
J20	SMA F	SMA M	LO-8	RG223	SMA M	LIJ10	SMA F
J21	SMA F	SMA M	RT1	RG223	SMA M	SIJ5	SMA F
J22	SMA F	SMA M	RT2	RG223	SMA M	SIJ11	SMA F
J23	SMA F	SMA M	RT3	RG223	SMA M	SIJ16	SMA F
J24	SMA F	SMA M	150 MHz	RG223	SMA M	FDJ9	SMA F
J25	SMA F	SMA M	180 MHz	RG223	SMA M	FDJ5	SMA F
J26	SMA F	SMA M	1 MHz	RG223	SMA M	FGJ10	SMA F
Mnemonic: RS							
Assembly Name: RF Switching Panel							
J1	25 Pin Female D Connector	Ansley 609-25P	Status & Control	Micro-Ribbon	Ansley 609-25S	WPJ5	25 Pin Male
J2	SMA Female	SMA M	XT1 Combiner 1	RG223	Male SMA	SIJ1	SMA F
J3	SMA Female	SMA M	XT1 Combiner 2	RG223	Male SMA	SIJ2	SMA F
J4	SMA Female	SMA M	XT2 Combiner 1	RG223	Male SMA	SIJ7	SMA F
J5	SMA Female	SMA M	XT2 Combiner 2	RG223	Male SMA	SIJ8	SMA F
J6	SMA Female	SMA M	XT3	RG223	Male SMA	SIJ13	SMA F
J7	SMA Female	SMA M	Transmitted RF	RG223	Male SMA	WPJ8	N Female

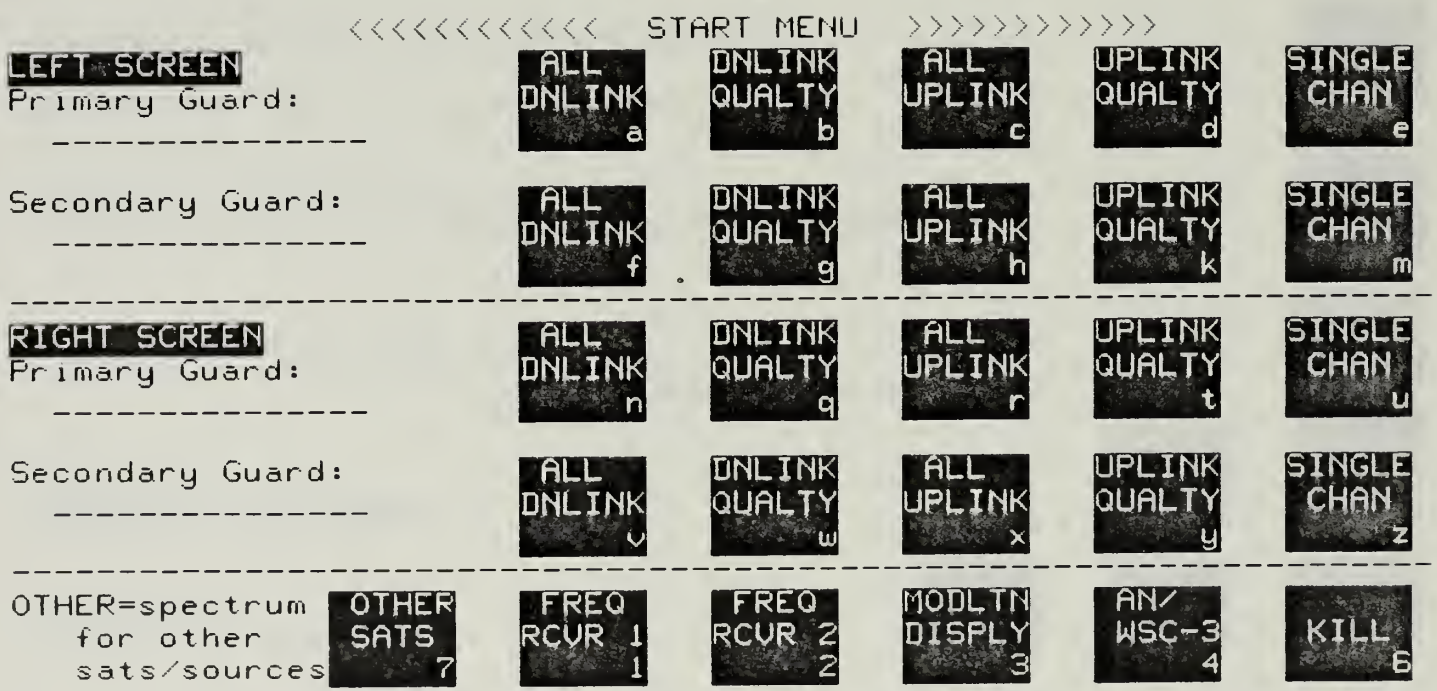
JACK	CONNECTOR	MATE	FUNCTION	CABLE	CONNECTOR	SOURCE & JACK	CONNECTOR ON SOURCE
Mnemonic: WP							
Assembly Name: WSC-3 Panel							
J1	MS3106A 22-19S	MS3106A 22-19P	DC Power				
J2	34 Pin PC Board Edge	Ansley 609-3415M	Interface	Micro-Ribbon	Ansley 609-3415M	TRJ7	34 Pin
J3	40 Pin Edge	Ansley 609-4015M	Interface	Micro-Ribbon	Ansley 609-25P	BE Data Interface	25 Pin Female
J4	MS3102A145-7S 3 Pin Amphenol	MS3106A 14S-7S	Audio	3-Wire Cable	MS3106A 14S-7S	ASJ5	MS3102A 7P
J5	25 Pin Male C Connector	Ansley 609-25S	Status/	Micro-Ribbon	Ansley 609-25P	RSJ1	25 Pin Female
J6	SMA Female	SMA M	Receive	RG223	SMA M	SSJ15	SMA Female
J7	SMA Female	SMA M	LO5	RG223	SMA M	LLJ15	
J8	Female N	Male N	RF Out	RG223	SMA M	RSJ7	SMA Female
J9	50 Pin PC Board Edge	Ansley 609-5015M	CBL-13	Micro-Ribbon	Ansley 609-5015M	CBL-13	50 Pin Edge
J10	MS3100A 4 Pin Amphenol	MS3106-A14S-2P	Noise Temp. Test	4-Wire Cable	MS3102A-125-3P	SIJ3J9J14 Single Cable	MS3102A-125-35
J11	16 Pin Edge	Ansley 609-1015M	Interface	Micro-Ribbon	Ansley 609-15S	DIJ1	15 Pin Male D
J12	Amphenol 57-40360	57-30360	Control		MS2746E21-B35P	RTJ2	MS27466E21-B35S
J13	Amphenol 57-40240	5730240	Control		MS3126F20-41P	RTJ3	MS3112E20-41S
J14	SMA Fem	SMA M	Ext MODEM	RG223	BNC M	RTJ5	BNC F
J15	SMA Fem	SMA M	Receive	RG223	Male N	RTJ9	Female N

JACK	CONNECTOR	MATE	FUNCTION	CABLE	CONNECTOR	SOURCE & JACK	CONNECTOR ON SOURCE
Mnemonic: WP [Continued]							
Assembly Name: WSC-3 Panel							
J16	Female N	Male N	Transmitted RF	RG223	Male N	RTJ8	Female N
J17	Amphenol 57-40500	Amphenol 57-30500	Freq Select	27 Pair E-20042	Discrete Wires	RT 1A1A20 P1	37 Pin D

APPENDIX G

TOUCH PANEL DISPLAYS AND INSTRUCTIONS TO CPU

The SSA operator interfaces with the SSA via the TOUCH PANEL. This appendix describes the use of the TEST UNIT through the displays observed by the operator on the TOUCH PANEL. Also included are specific instructions to the CPU required to implement TEST UNIT functions.


<<<<<<<<<<<< START MENU >>>>>>>>>>>>
LEFT SCREEN
Primary Guard:

ALL DNLINK a
DNLINK QUALTY b
ALL UPLINK c
UPLINK QUALTY d
SINGLE CHAN e
Secondary Guard:

ALL DNLINK f
DNLINK QUALTY g
ALL UPLINK h
UPLINK QUALTY k
SINGLE CHAN m
RIGHT SCREEN
Primary Guard:

ALL DNLINK n
DNLINK QUALTY q
ALL UPLINK r
UPLINK QUALTY t
SINGLE CHAN u
Secondary Guard:

ALL DNLINK v
DNLINK QUALTY w
ALL UPLINK x
UPLINK QUALTY y
SINGLE CHAN z
OTHER=spectrum for other sats/sources
OTHER SATS 7
FREQ RCVR 1 1
FREQ RCVR 2 2
MODLTN DISPLY 3
AN/ WSC-3 4
KILL 6

ctrl099 - KILL MENU

KILL AN/WSC-3 XMTR

KILL WSC-3 a

KILL RCVR TEST SIGNAL

KILL TEST b

PREV MENU p

task020 - SYSTEM TEST and CALIBRATION

SELECT the TEST you wish to perform.

OPERATING TEMPERATURE

AN/WSC-3 TRANSMITTER TEST

SELF TEST
INTERIM TEST SIGNAL

CALIBRATION
INTERIM CALIBRATION

task 060 - INTERIM CALIBRATION

Select CALIBRATION to be entered.

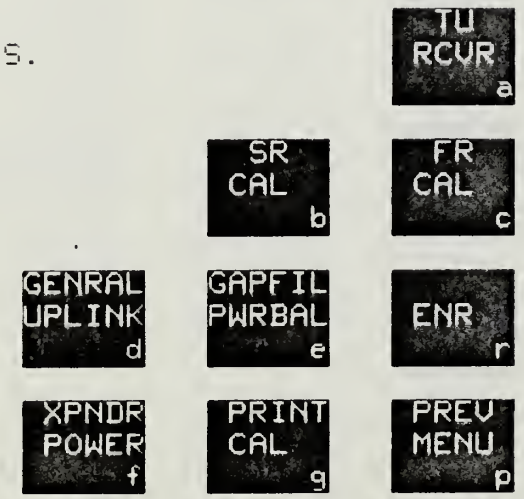
TEST UNIT (RCVR TEST)
** MUST BE DONE PRIOR TO TESTING RECEIVERS.

SPECTRUM RECEIVERS (SR)
FREQUENCY RECEIVERS (FR)

TEST UNIT (AN/WSC-3 XMTR):
   GENERAL UPLINK
   GAPFILLER POWER BALANCE
EXCESS NOISE RATIO

TRANSPONDER POWER

PRINT CAL = Print all CALIBRATION FACTORS



task061 - INTERIM CALIBRATION - TEST UNIT RCVR (1)

Select the ANTENNA for entry
of the TEST UNIT RECEIVER
CALIBRATION FACTOR.

ANTENNA

ANT 1
1

ANT 2
2

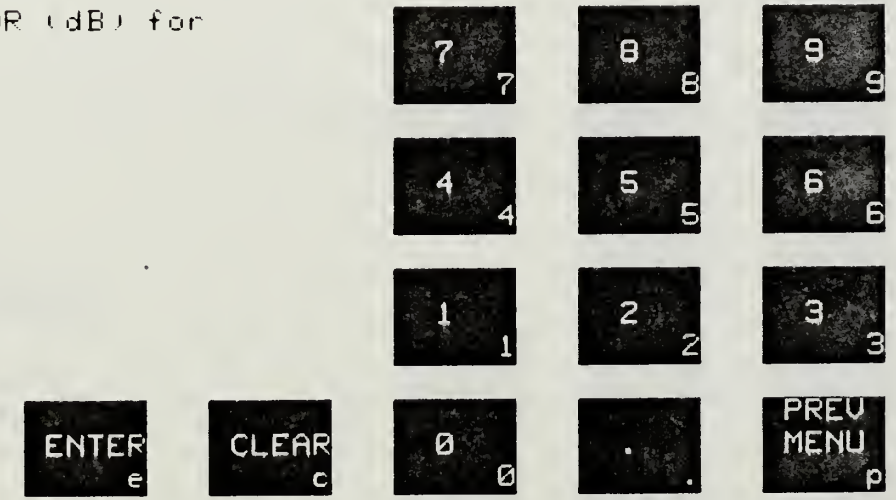
ANT 3
3

PREV
MENU
p

task062 - INTERIM CALIBRATION - TEST UNIT RCVR TEST (2)

Enter CALIBRATION FACTOR (dB) for

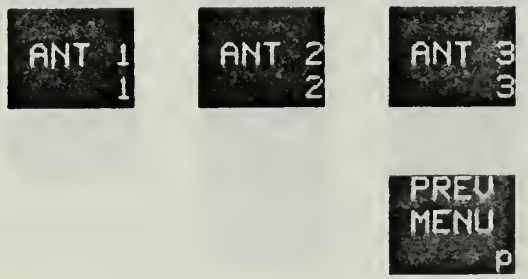
ANTENNA __



task063 - INTERIM CALIBRATION - EXCESS NOISE COUPLING LOSS

Select the ANTENNA for entry
of the EXCESS NOISE RATIO (ENR)
and the COUPLING LOSS.

ANTENNA

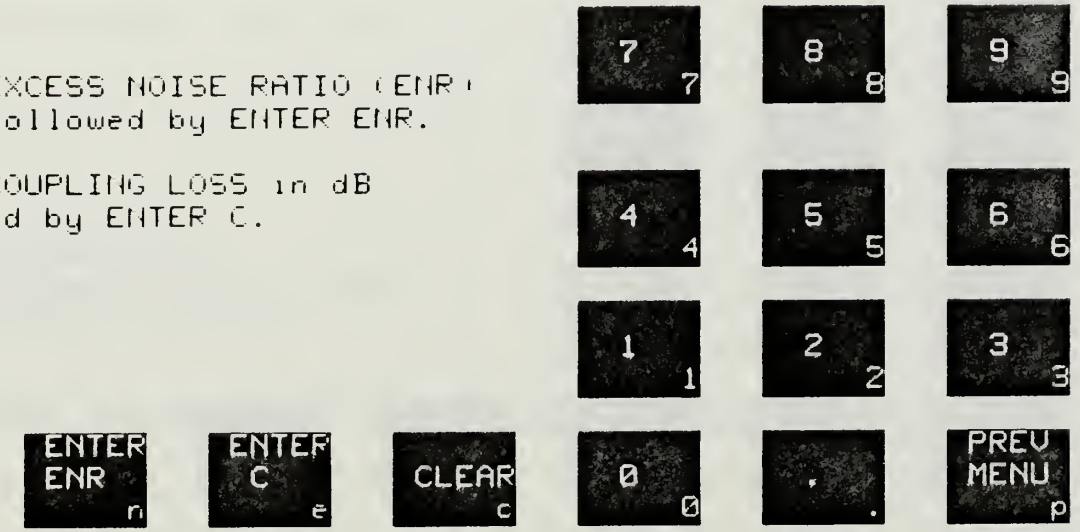


task069 - INTERIM CALIBRATION - EXCESS NOISE RATIO COUPLING LOSS

For ANTENNA _

1. Enter EXCESS NOISE RATIO (ENR) in dB followed by ENTER ENR.

2. Enter COUPLING LOSS in dB followed by ENTER C.



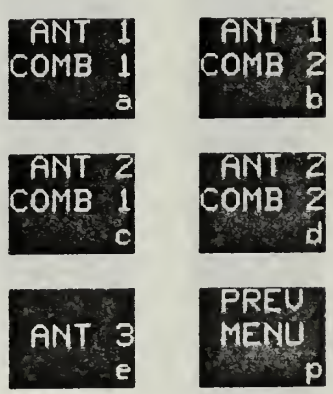
task070 - INTERIM CAL - TEST UNIT (AN/WSC-3 XMTR) - GENRL UPLINK (1)

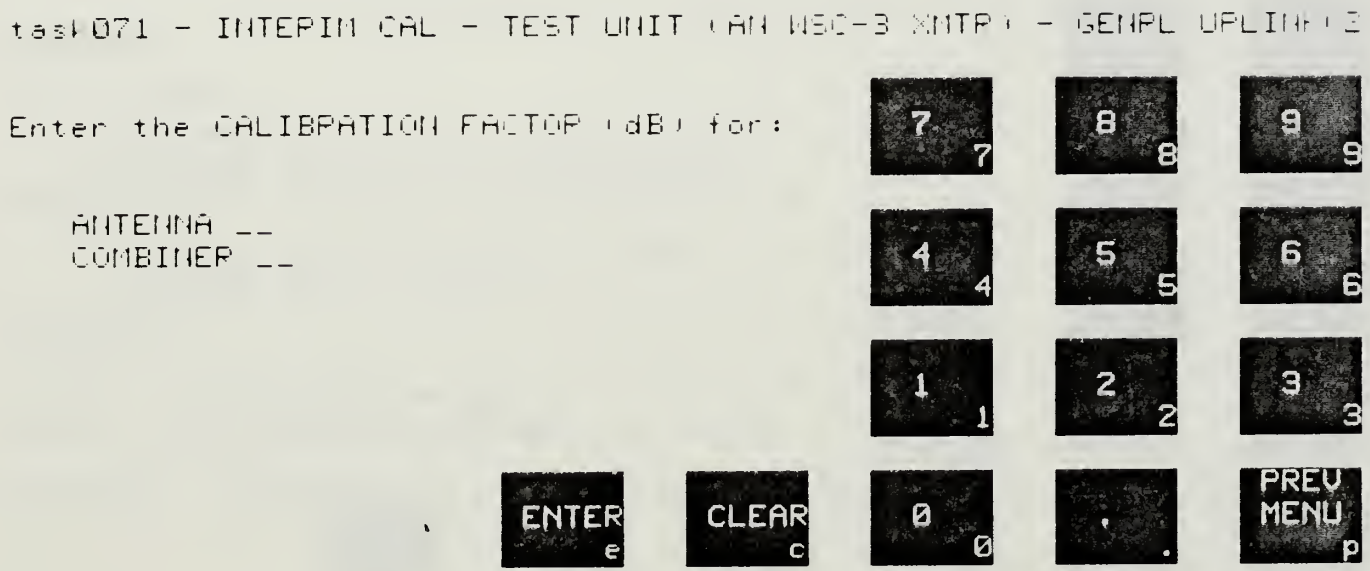
Select the ANTENNA/COMBINER for entry
of CALIBRATION FACTOR.

ANTENNA 1
combiner 1
combiner 2

ANTENNA 2
combiner 1
combiner 2

ANTENNA 3




task 071 - INTERIM CAL - TEST UNIT (AN WSC-3 XMTR) - GENRL UPLINK (3)
Enter the CALIBRATION FACTOR (dB) for:
ANTENNA __
COMBINER __
7 7
8 8
9 9
4 4
5 5
6 6
1 1
2 2
3 3
ENTER e
CLEAR c
0 0
. .
PREV MENU p

task073 - INTERIM CAL- TEST UNIT (AN WSC-3 XMTR) - GAPFILLER PBAL(1)
Select the ANTENNA/COMBINER
for entry of CALIBRATION FACTOR.

Antenna 1
  combiner 1
  combiner 2

Antenna 2
  Combiner 1
  Combiner 2

Antenna 3

ANT 1 COMB 1 a

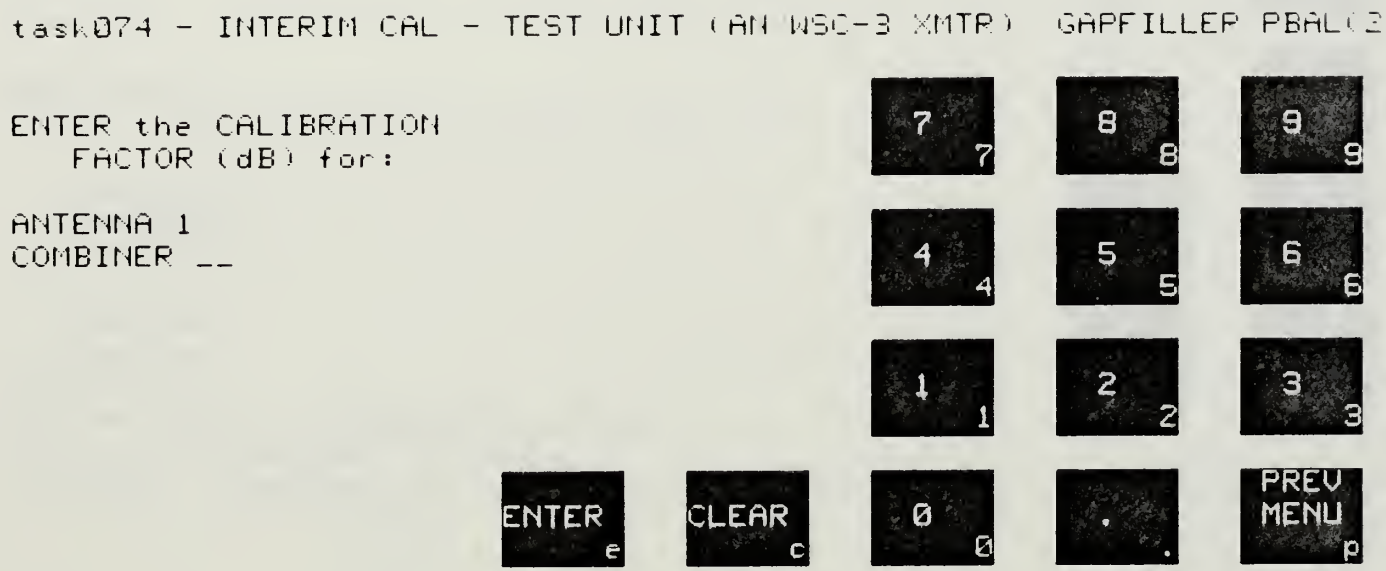
ANT 1 COMB 2 b

ANT 2 COMB 1 c

ANT 2 COMB 2 d

ANT 3 e

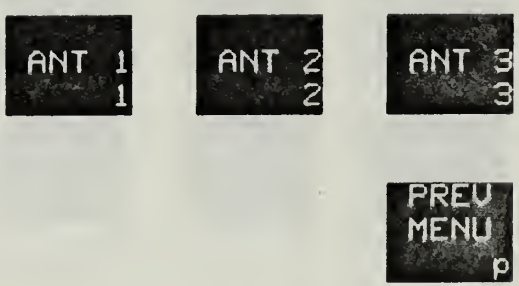
PREV MENU p


task074 - INTERIM CAL - TEST UNIT (AN WSC-3 XMTR) GAPFILLER PBAL(2)
ENTER the CALIBRATION
FACTOR (dB) for:
ANTENNA 1
COMBINER __
7 7
8 8
9 9
4 4
5 5
6 6
1 1
2 2
3 3
ENTER e
CLEAR c
0 0
. .
PREV MENU p

task076 INTERIM CALIBRATION - TRANSPONDER POWER (1)

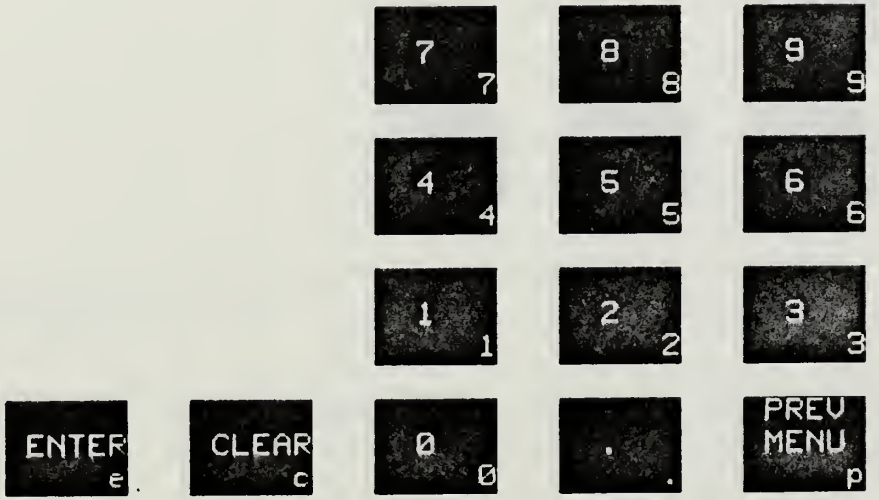
Select the ANTENNA for entry
of TRANSPONDER CALIBRATION FACTOR.

Antenna



task077 Interim Calibration - TRANSPONDER POWER (2)

Enter the CALIBRATION
FACTOR (dB) for:
ANTENNA __



Instructions to CPU for INTERIM CALIBRATION

Receiver Test Calibration (TASK 061, 062)

The operator enters a calibration factor in dB on a keypad display on Task 062. Previously, on Task 061, he defined the antenna chain to which his entry applies.

The calibration factor he enters is the cable/coupling loss from the Receiver Test Section to the antenna RF preamplifier.

During SSA operation, the operator will specify a desired power level for Receiver Test Signals. CBL12 controls an attenuator in the test signal path. The amount of attenuation needed will be the difference between the calibration factor and the desired power level.

e.g.

Cal. factor = -63 dB

Desired power = -93 dBm

Attenuation = 30 dB

AN/WSC-3 TRANSMIT (TASK 070,071)

The operator enters a calibration factor in dB with a keypad display on Task 071. Previously, with a display on 070, the operator enters the antenna/combiner combination to which his entry applies.

The calibration factor he enters corrects for the cable/coupling loss plus antenna gain between the output of the transmitter to EIRP at the antenna.

AN/WSC-3 TRANSMIT (TASK 070, 071) (continue)

During normal SSA operation, the operator will specify desired EIRP for AN/WSC-3 transmit signals. CBL11 provides a power command to the High Power Leveler. The CPU must determine the power command needed for the desired EIRP.

Power Command = EIRP - (Calibration factor + K)

where K is the difference between commanded power and resulting power out of the AN/WSC-3. K is provided in form of a table look up. The quantity in brackets is rounded to the nearest dB.

Power Command (dBW)	Resulting Power (dBW)
0	0.1
1	1.1
2	2.1
3	3.0
4	4.0
5	5.0
6	6.0
7	7.0
8	8.2
9	9.1
10	10.1
11	11.1
12	12.0
13	13.0

AN/WSC-3 TRANSMIT (TASK 070, 071) (continue)

Power Command (dBW)	Resulting Power (dBW)
14	14.0
15	15.0
16	16.1
17	17.1
18	18.1
19	19.0
20	20.0

Gapfiller Power Balance (TASK 073, 074)

The operator enters a calibration factor in dB with a keypad displayed on TASK 074, for the antenna/combiner combination selected on TASK 073.

The calibration factor is the difference between a selected power command (say, 20 dBW) and the measured EIRP for the antenna/combiner chosen. This factor should be stored in a look-up table for use during power balance calibrations.

Transponder Power (TASK 076, 077)

The operator enters a calibration factor with a keypad displayed on TASK 077, for the antenna chosen on TASK 076.

This calibration factor is the sum of free space loss, antenna gain and losses; it is used in determination of satellite power.

Transponder Power (TASK 076, 077) (continue)

$C = EIRP + Lfs + Gr + Lo$

$CALIBRATION\ FACTOR = Lfs + Gr + Lo$

$C = EIRP + CALIBRATION\ FACTOR$

Operating Temperature

Operator enters antenna, then two calibration factors: one is the excess noise ratio (ENR) of the noise diode; the other is the coupling loss from the output of the noise diode to the input of the RF preamplifier.

CPU must calculate T_E

C and ENR are entered in dB.

task030 - INTERIM TEST SIGNAL

This test injects a signal with adjustable characteristics in the RF deck box.

Select ANTENNA.

Select MODULATION. (bps)

Enter or change FREQUENCY POWER LEVEL.

Select DATA SOURCE: NORM DEA

To START test:

1. Push START TEST.
2. Push POWER ENABLE on TEST UNIT within 15 seconds.

task031 - INTERIM SIGNAL TEST

Select FREQUENCY (in MHz) using keypad.

Use buttons as keypad.

MISTAKE?
Press CLEAR and start again.

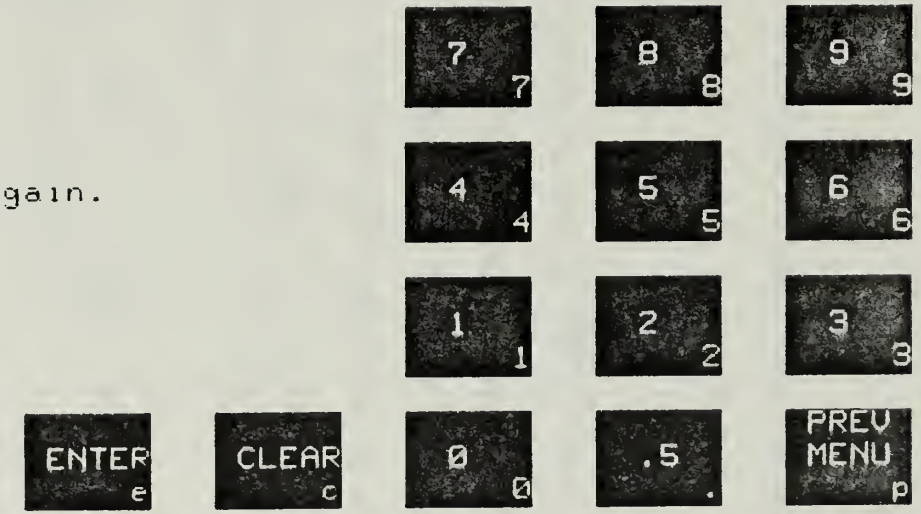
Press ENTER when done.

task032 - INTERIM SIGNAL TEST
Select POWER LEVEL (-dBm).
    The highest power available is
    -50dBm; lowest is -130dBm.

Use buttons as keypad.

MISTAKE?
Press CLEAR and start again.

Press ENTER when done.



Instructions for Interim Signal Test (IST)

1. When IST is selected, CLB12, byte 2, bit 0 goes high to enable Rcvr Test.

2. Antenna selection; CBL12, byte 2

   bit 7 H = ant 3

   bit 6 H = ant 2

   bit 5 H = ant 1

3. Modulation Select: CBL12, byte 3.

   bit 7. High = PSK LOW = CW

   Data rate is selected via bits 6 - 4:

D6	D5	D4		
0	0	0	=	75
0	0	1	=	300
0	1	0	=	600
0	1	1	=	1200
1	0	0	=	2400
1	0	1	=	4800
1	1	0	=	9600
1	1	1	=	19.2 K

4. Frequency select: Local Osc. 8 is mixed with 150 MHz to provide desired frequency. Allow a 50 usec WAIT between frequency change and measurement.

5. Power select. With no attenuation, power at antenna due to RCVR Test is equal to the calibration factor.

Instructions for Interim Signal Test (IST) (cont.)

Attenuators provide .5 dB increments of attenuation from .5 to 95.5 dB

Attenuation

CBL 12 Byte 1

Bit:	7	6	5	4	3	2	1	0
Atten:	32	32	16	8	4	2	1	.5

The difference between calibration factor and whatever the operator selects for power level is the amount of desired attenuation. Calibration factor is entered during interim calibration.

6. CBL12 Byte 2, bit 1 turns the TEST ON and OFF after the enable sequence is completed.

START TEST and STOP TEST control this bit as long as operator is on this menu.

task040 AN/WSC-3 TRANSMITTER TEST - COMPUTER CONTROLLED

This test checks the settings of the AN WSC-3 and checks if it is transmitting RF power when keyed. The AN WSC-3 is connected to DUMMY LOAD during this test.

AN/WSC-3 set-up:	TEST KEY - OFF
POWER METER - HIGH	FREQ SELECT - PRESET
SATCOM/LOS - LOS	OPERATE/STANDBY - OPERATE
REMOTE/LOCAL - REMOTE	PRIMARY POWER - ON

(Note that these are the normal settings for all operations of the AN/WSC-3 under SSA control.)

1. Enable the test by pushing XMTR ENABLE on the TEST UNIT.
2. Start the test by pushing the RUN button below.
3. Observe the power meter on the AN/WSC-3. It should read approximately 20 dBW.
4. TEST will automatically be DISABLED when you leave this menu.

RUN r STOP h PREV MENU p

HELP MENU

AN/WSC-3 Transmit Test (Task 040)

The purpose of this test is to check proper set-up of the AN/WSC-3 and to verify that it is indeed transmitting RF power when keyed.

The set-up instructions list the AN/WSC-3 settings that are required if the AN/WSC-3 is to be used under SSA control. If these settings are not made, the SSA cannot properly control the AN/WSC-3.

The XMTR ENABLE button is located on the Test Unit panel. This button enables the AN/WSC-3.

The AN/WSC-3 is not keyed until the RUN button on the Touch Panel is selected, and the XMTR ENABLE button is pushed.

Instructions to CPU for XMTR TEST (TASK 040)

When the operator chooses RUN, CBL12, Byte 2, bits 2 and 3 must be raised to HIGH (5) levels to enable the WSC-3. If the "RF above 1 watt" status is not ON within 5 seconds, turn these bits off.

Additionally CBL11 is latched as follows to provide frequency, modulation and power control:

Byte 3, Bit 3-7.

need 20 dB of attenuation to set up for 20 dBW transmit.

Byte 2, Bit 6

LOW for CW

Byte 0 and 1. BCD frequency control.

Set up 300 MHz.

ctrl050 - AN/WSC-3

TO STOP TRANSMITTER

STOP XMIT x

You may use the AN/WSC-3 to:

1. Transmit CW or PSK
2. Receive AM, FM, FSK, or PSK

Set-up for AN/WSC-3:

Primary power - ON
Operate/Standby - OPERATE
RF Power Meter - HIGH
Test Key - OFF
Satcom/LOS - LOS
Remote/Local - REMOTE
Freq. Select - PRESET

Set up TRANSMIT or RECEIVE:
(Instructions will follow.)

XMIT t RCV r PREV MENU p

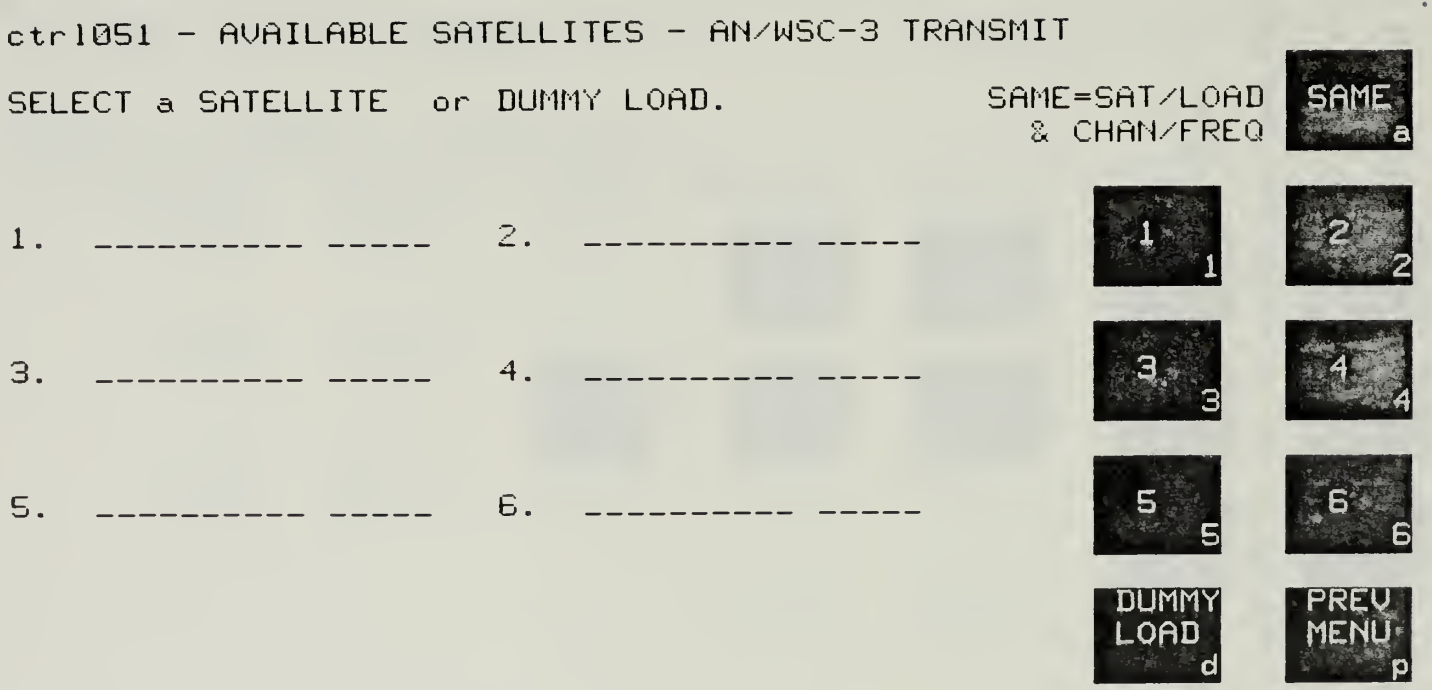
HELP MENU

WSC-3 (Ctrl 050)

The STOP XMIT button may be used to stop the transmitter and disable the RF keyline. It is provided in the event the operator wants to use the AN/WSC-3, finds that it is currently transmitting, and wants to stop the transmitter before proceeding.

The set-up instructions list the AN/WSC-3 settings that are required if the AN/WSC-3 is to be used under SSA control. If these settings are not made, the SSA cannot properly control the AN/WSC-3.

The XMIT and RCV buttons are used to select transmit or receive. The displays and instructions are different for each, so the operator must first choose which function he desired to perform.


ctrl051 - AVAILABLE SATELLITES - AN/WSC-3 TRANSMIT
SELECT a SATELLITE or DUMMY LOAD.
SAME=SAT/LOAD & CHAN/FREQ
SAME a
1. ---------- -----
2. ---------- -----
1 1
2 2
3. ---------- -----
4. ---------- -----
3 3
4 4
5. ---------- -----
6. ---------- -----
5 5
6 6
DUMMY LOAD d
PREV MENU p

HELP MENU

WSC-3 Source Selection (Ctrl 051)

Six sources are listed on the display and labeled with a number. Corresponding to each source is a button with the same number. Touching one of these buttons results in the selection of the source with the same label.

ctrl052 FLTSATCOM CHANNEL SELECT AN/WSC-3 TRANSMIT

Select a CHANNEL or FREQ SELECT.
FREQ SELECT allows choice of a specific frequency.

HELP MENU

WSC-3 XMIT FLTSAT Channel/Frequency Select (Ctrl 052)

The operator may choose one of the Navy FLTSAT channels listed or he may choose to specify a certain frequency.

If one of the channels is selected, the AN/WSC-3 will automatically be tuned to that channel.

If a specific frequency is desired a new display will appear, permitting the operator to choose his frequency.

ctrl053 - GAPFILLER CHANNEL SELECT AN/WSC-3 TRANSMIT

Select a CHANNEL or FREQ SELECT.
FREQ SELECT allows choice of a specific frequency.

WB = WIDEBAND
NB = NARROWBAND

HELP MENU

WSC-3 XMIT Gapfiller Channel Select (Ctrl 053)

The operator may choose one of the GAPFILLER channels or selection of a specific frequency may be chosen.

If one of the channels is selected, the AN/WSC-3 will be automatically tuned to that channel.

If a specific frequency is desired, a new display will appear, permitting the operator to choose his frequency.

ctrl058 - FREQUENCY SELECT

AN/WSC-3 TRANSMIT

Select UPLINK FREQUENCY (in MHz).
  292 - 312 MHz = Uplink

Use buttons as keypad.
Decimal point must be used.

MISTAKE?
Press CLEAR and start again.

Press ENTER when done.

HELP MENU

WSC-3 XMIT Frequency Select (Ctrl 058)

The buttons are used as a keypad to enter frequency in MHz. The decimal point must always be used, even if the desired frequency is an integer number of MHz.

For example, to enter 307 MHz, the following sequence of buttons is selected:

3 0 7 . ENTER

ctrl059 AN/WSC-3 TRANSMITTER MODULATION SELECT

Select MODULATION.

DATA SOURCE for PSK
(DEA = HP1645A DATA ERROR ANALYZER)

Select COMBINER (omit if using antenna 3).

HELP MENU

WSC-3 XMIT Modulation Select (Ctrl 059)

In the SSA, the AN/WSC-3 may be used to transmit CW or PSK. The permissable PSK data rates are 75 bps, 300 bps, 1200 bps, 2400 bps, 4800 bps and 9600 bps.

There are two sources of data for PSK modulation.

1. A pseudo-random sequence generator, of length 511, is built into the SSA. This is the normal source of PSK data for SSA operation.
2. The HP1645A Data Error Analyzer may be used to provide a pseudo-random data sequence of various lengths, selected by the operator. The HP1645A should be used as a data source only for calibration or troubleshooting.

One of two combiners must be selected if the AN/WSC-3 is transmitting over the same antenna(s) as the AN/WSC-5's. (This selection is ommitted if the SSA antenna is used.) Combiner selection depends upon which channel is being utilized; each channel is assigned to a specific combiner.

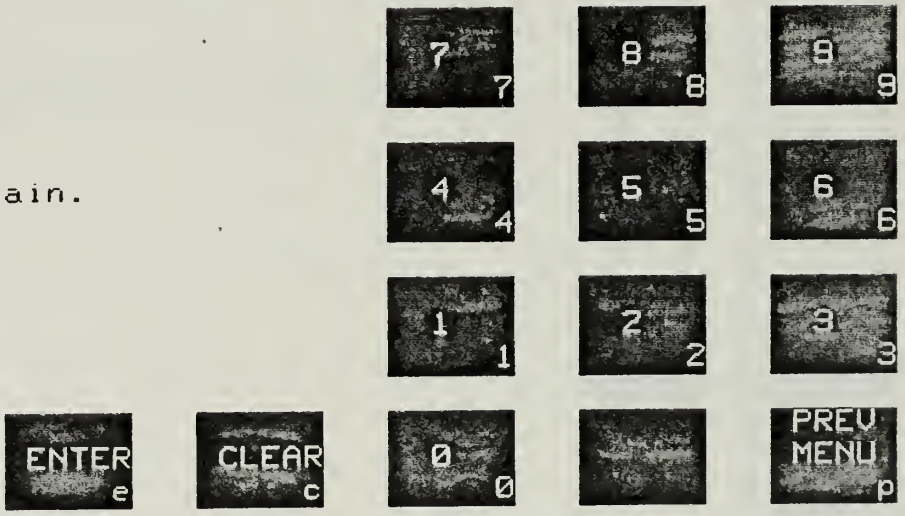
ctrl060 - AN/WSC-3 EIRP POWER LEVEL

Enter desired EIRP power level,
in dBW, on keypad.

Use buttons as keypad.

MISTAKE?
Press CLEAR and start again.

Press ENTER when done.



HELP MENU

WSC-3 XMIT Power Level (Ctrl 060)

Enter desired EIRP in decibels. EIRP is the power out of the antenna--not out of the AN/WSC-3. EIRP equals power out of AN/WSC-3 minus cable loss plus antenna gain. The AN/WSC-3 will be programmed to provide on actual transmit power that will result in the desired EIRP.

ctrl061 - AN/WSC-3 TRANSMIT

To TRANSMIT:

1. Push XMIT below.

2. Push XMTR ENABLE button on TEST UNIT within 5 seconds.

To HALT TRANSMISSION:

1. Push STOP.

HELP MENU

WSC-3 XMIT (Ctrl 061)

Two actions are now required to transmit.

1. Touch the XMIT button on the Touch Panel.

2. Push the XMTR ENABLE button on the Test Unit panel (within five seconds of touching the XMIT button).

The STOP button halts transmission.

If STOP has been selected or if five seconds elapse between selecting XMIT and XMTR ENABLE, both steps (1) and (2) above must be repeated in order to transmit again.

Instructions to CPU for AN/WSC-3 Transmit

1. Frequency control is same as for receive with two exceptions.

a. The computer must sense whether XMIT or RCV has been chosen. When a channel is selected, the frequency that is used depends upon whether transmitting or receiving. See frequency plan.

b. LO5 is programmed to 70+Δ MHz vice 90+Δ MHz.

2. Antenna selection. AN/WSC-3 RF output power is routed to the selected antenna via WP and RS. Control is from CBL11, byte 2, bits 0, 1, and 2.

Bit 0. LOW = Combiner 1

HIGH = Combiner 2

Bits	2	1		
	0	0	Dummy Load	
	0	1	Ant. 1	Positive Logic
	1	0	Ant. 2	
	1	1	Ant. 3	

3. Power Control. CBL11 byte 3 bit 3-7

Bit		
7 = 16 dB		
6 = 8 dB		
5 = 4 dB	Choose so that sum equals	
4 = 2 dB	power command.	
3 = 1 dB		

Allow a 5 msec. wait between power selection and the conduct of any measurement.

Instructions to CPU for AN/Wsc-3 Transmit (cont.)

4. Modulation. CW - byte 2, bit 6 LOW; PSK - byte 2, bit 6 HIGH. Byte 2, bit 7 HIGH selects DEA for PSK data; LOW selects internal data.

Bits	5	4	3	PSK data rate
	0	0	0	75 bps
	0	0	1	300 bps
	0	1	0	600 bps
	0	1	1	1200 bps
	1	0	0	2400 bps
	1	0	1	4800 bps
	1	1	0	9600 bps
	1	1	1	19.2k bps

5. To key the transmitter: When RUN is pushed, CBL12 byte 2 bits 2 and 3 go HIGH. If STOP is pushed, these bits go LOW; the transmitter is off.

6. If AN/WSC-3 is in LOCAL mode, LO5 should be programmed to 90.000 MHz.

ctrl071 - AVAILABLE SATELLITES AND SOURCES AN/WSC-3 RECEIVE

SELECT the SATELLITE or SOURCE
you wish to MONITOR.

SAME=SAT/SOURCE
& CHAN/FREQ

SAME d

1. _____ _____ 2. _____ _____

1 1 2 2

3. _____ _____ 4. _____ _____

3 3 4 4

5. _____ _____ 6. _____ _____

5 5 6 6

OTHER SOURCES

ANT 1 a ANT 2 b ANT 3 c TAPE PLAY t PREV MENU p

HELP MENU

Available Satellites and Sources (Ctrl 071)

Six sources are listed on display and labeled with a number. Corresponding to each source is a button with the same number. Touching one of these buttons results in the selection of the source with the same label.

ctrl072 FLTSATCOM CHANNEL SELECT AN/WSC-3 RECEIVE

Select a CHANNEL or FREQ SELECT.
FREQ SELECT allows choice of a specific frequency.

HELP MENU

WSC-3 RCV FLTSAT Channel Select (Ctrl 072)

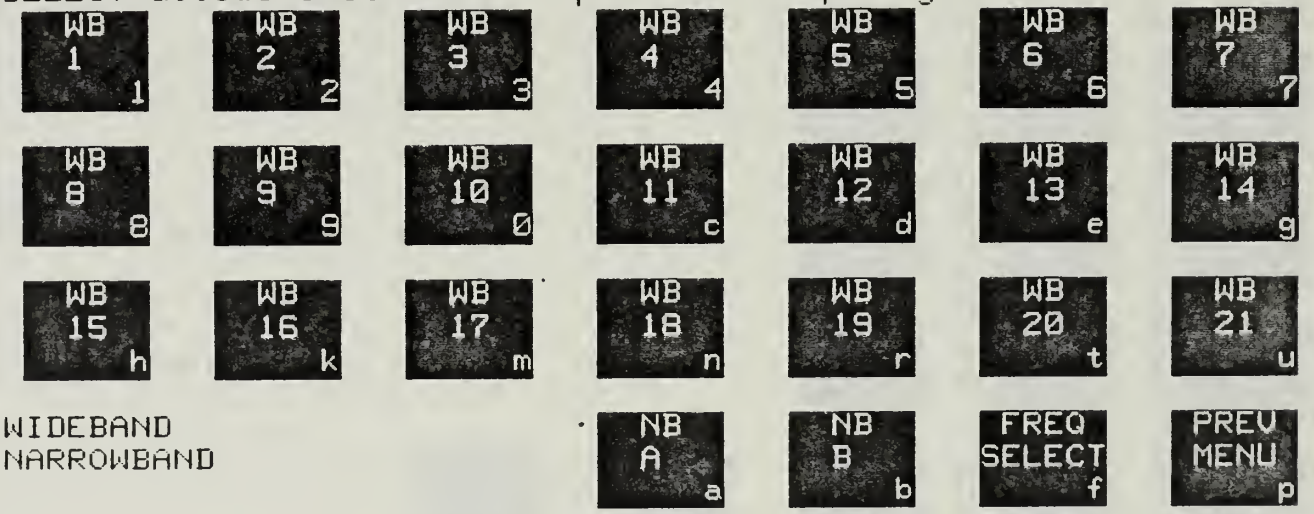
The operator may choose one of the Navy FLTSAT channels or a specific frequency may be selected.

If one of the channels is selected, the AN/WSC-3 will automatically be tuned to that channel.

If a specific frequency is desired a new display will appear, permitting the operator to choose his frequency.

ctrl073 - GAPFILLER CHANNEL SELECT AN/WSC-3 RECEIVE

Select a CHANNEL or FREQ SELECT.
FREQ SELECT allows choice of a specific frequency.



WB = WIDEBAND
NB = NARROWBAND

HELP MENU

WSC-3 RCV GAPFILLER Channel Select (Ctrl 073)

The operator may choose one of the NAVY GAPFILLER channels, or a specific frequency may be selected.

If one of the channels is selected, the AN/WSC-3 will automatically be tuned to that channel.

If a specific frequency is desired, a new display will appear, permitting the operator to choose his frequency.

ctrl078 - FREQUENCY SELECT AN/WSC-3 RECEIVE

Select FREQUENCY (in MHz).
240 - 270 MHz = Downlink

Use buttons as keypad.
Decimal point must be used.

MISTAKE?
Press CLEAR and start again.

Press ENTER when done.

WSC-3 RCV Frequency Select (Ctrl 078)

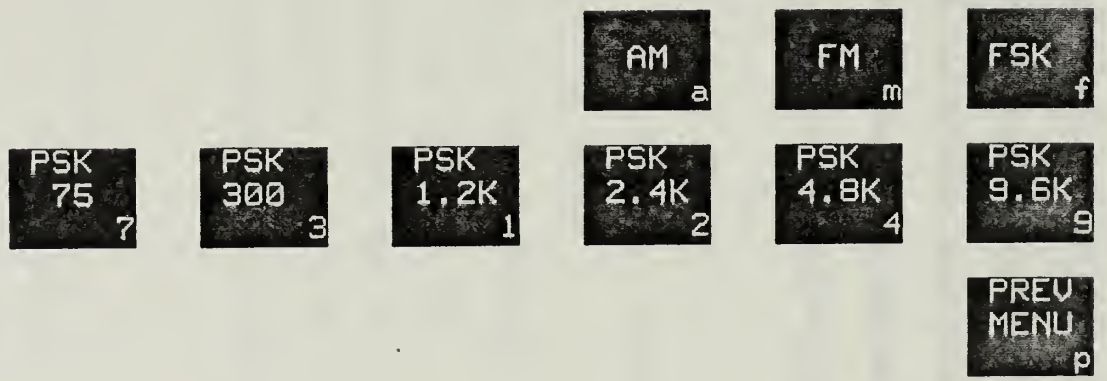
The buttons are used as a keypad to enter frequency in MHz. The decimal point must always be used, even if the desired frequency is an integer number of MHz.

For example, to enter 247 MHz, the following sequence of buttons is selected:

2 4 7 . ENTER

ctrl079 AN/WSC-3 RECEIVER DEMODULATION SELECT

Select DEMODULATION mode:



WSC-3 RCV Demodulation Mode (Ctrl 079)

In the SSA, the AN/WSC-3 may be used to receive AM, FM, FSK or PSK. The permissible PSK data rates are: 75 bps, 300 bps, 1200 bps, 2400 bps, 4800 bps, 9600 bps.

One of these demodulation modes must be selected by touching the corresponding button on the touch panel.

Instructions to CPU for AN/WSC-3 Receive

1. Route signal from source to WSC-3 via Signal Selector.

2. WSC-3 frequency is controlled by CBL11, Byte 1, Bits 0-7 and Byte 0, Bits 1-7. Frequency is established by channel selection or by precise frequency selection menus. AN/WSC-3 frequency may be adjusted to 25 kHz resolution, i.e. $300.\begin{matrix}00\\25\\50\\75\end{matrix}$. More precise frequency resolution is obtained via the Local Oscillator (LO #5).

a. Find the offset or difference (Δ) between desired frequency and the nearest 25 kHz center.

b. Program LO #5 to $90\pm\Delta/2$ MHz as needed. LO frequency is doubled on the WP panel to give $180\pm\Delta$ MHz.

3. Demodulation mode: CBL11 Byte 3, bit 0, 1, 2 and Byte 0 bit 0. To select AM, make Byte 3, bits 0, 1, 2 LOW and make Byte 0 bit 0 HIGH. To select others, make Byte 0, bit 0 LOW and:

Byte 3 Bit	2	1	0	
	0	0	0	PSK 75
	0	0	0	PSK 300
	0	1	0	PSK 1200
	0	1	1	PSK 2400
	1	0	0	PSK 4800
	1	0	1	PSK 9600
	1	1	0	FSK
	1	1	1	FM

task021 - OPERATING TEMPERATURE

STANDARD TEST

MANUAL TEST

HELP MENU

Operating Temperature Manual Test (Task 021)

The standard test utilizes the SSA array processor to automatically calculate operating temperature down thru each of the three RF chains from RF preamplifiers (at antennas) to output of the RF units.

In the Manual Test, the operator observes the change in output noise power on the Test Unit spectrum analyzer. This change is called the Y-factor. The operator will then be required to enter his observed Y-factor as input to the CPU. The computer will calculate and display the resulting operating temperature. In the manual test, operating temperature may be calculated down thru system RF output or IF output as desired. Succeeding displays prompt the operator as to how to proceed.

task022 - OPERATING TEMPERATURE - MANUAL TEST (1)

In this test the operator uses the Tektronix 7L12 to observe changes in noise level due to injection of a known amount of noise at the antenna. The computer will then calculate the operating temperature.

To test noise temperature down thru RF press RF.

To test noise temperature down thru IF press IF.

Select ANTENNA.

RF r

IF f

ANT 1 1

ANT 2 2

ANT 3 3

NEXT MENU n

PREV MENU p

HELP MENU

Operating Temperature Manual Test (Task 022)

The operator may check operating temperature down through RF unit output by selecting RF or down through IF output by selecting IF.

The desired antenna is selected next. In the manual test, operating temperature is calculated for one antenna chain at a time. To check all antenna chains manually, the test must be repeated for each antenna.

task023 - OPERATING TEMPERATURE - MANUAL TEST (2)

Set controls on the Tektronix scope as follows:

VERT MODE- RIGHT	RF - 0dB ATTENUATION
TRIG SOURCE - RIGHT	REFERENCE LEVEL - 30dBm
START/CENTER - CENTER	TIME/DIV - "SPECTRUM"
FREE RUN - IN	NORM - IN
VIDEO FILTER - 3Hz	REF VAR - FULLY COUNTERCLOCKWISE
VIDEO PROCESSOR - OUT	FREQ/DIV - 50 kHz
RESOLUTION - 300kHz	LOG - 10 dB/DIV
BASELINE CLIPPER - FULLY COUNTERCLOCKWISE	

On the TEST UNIT panel set:
Spectrum Analyzer attenuation - 0dB

To CONTINUE press NEXT MENU.

NEXT MENU n

PREV MENU p

HELP MENU

Operating Temperature Manual Test (Task 023)

This set of instructions ensures that the Tektronix spectrum analyzer in the Test Unit is properly set. Each word on the display corresponds to a different control knob or button that can be found either on the Tektronix 7613 mainframe or 7L12 spectrum analyzer plug-in unit.

task024 OPERATING TEMPERATURE - MANUAL TEST(3)

Tune Spectrum Analyzer to ___.000MHz.

Set frequency marker on TEST UNIT to ___.000MHz.

Turn MARKER ON.

Using the "coarse" and "fine" knobs, adjust the spectrum analyzer so the marker appears in the center of the display.

Turn marker OFF.

Select the _____ pushbutton.
on the TEST UNIT.

NEXT MENU n

PREV MENU p

HELP MENU

Operating Temperature Manual Test (Task 024)

The spectrum analyzer frequency must be tuned to either 247 MHz or 67 MHz to observe the change in output noise power. For RF, use 247 MHz; for IF, use 67 MHz.

The frequency tuner on the spectrum analyzer is used to get the display close to the desired frequency.

The Test Unit Marker Frequency is used to get the spectrum analyzer display centered precisely on the appropriate frequency.

After the spectrum analyzer is properly tuned, the desired signal must be selected by pushing the pushbutton indicated. The pushbutton is found at the top of the right side of the Test Unit panel.

task 025 OPERATING TEMPERATURE - MANUAL TEST (4)

1. Observe the noise level on the Tektronix scope.

2. Push the RUN button below.

3. Note the CHANGE in noise level (in dB).
   The next display allows you to enter this CHANGE.
   Operating Temperature will be calculated and displayed.

4. Select REPEAT to repeat your measurement. Return to step 1.

5. Select NEXT if ready for Operating Temperature calculation.

RUN r

REPEAT t

NEXT MENU n

PREV MENU p

HELP MENU

Operating Temperature Manual Test (Task 025)

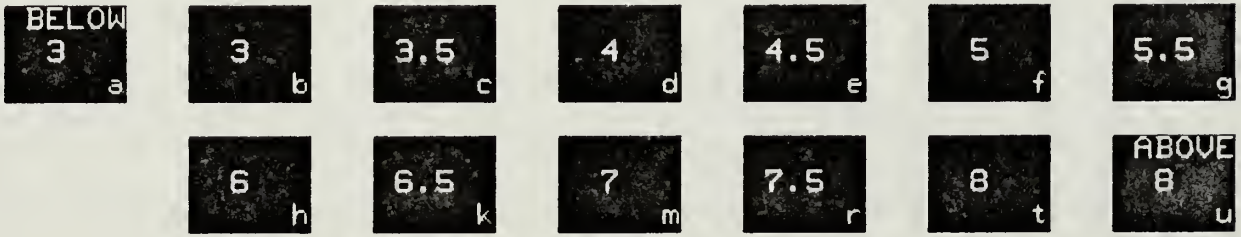
The RUN button activates a noise generator in the antenna deck box. Touching it will cause the noise level on the spectrum analyzer to rise a few dB.

The RESET button turns the noise generator off. The operator may select between RUN and RESET as desired.

When the operator is ready for the computer to calculate operating temperature, he should record the change in noise level, to 1/2 dB then select NEXT MENU.

task 026 OPERATING TEMPERATURE - MANUAL TEST (5)

Enter observed CHANGE in noise level in dB:



The NOISE TEMPERATURE in KELVINS will be printed on the printer.

HELP MENU

Operating Temperature Manual Test (Task 026)

Select the button that is nearest the observed change in output noise level.

If the change was less than two dB or more than seven dB there may be a fault either in the system hardware or in the operating temperature test.

The noise temperature, in degrees Kelvin, will be displayed on the printer keyboard.

Instructions to CPU for OPERATING TEMPERATURE TEST

When RUN is pushed, CBL12, Byte 3, bit 1, 2 or 3 (for antenna 1, 2 or 3 respectively) must go low (0 VDC) to enable the appropriate noise diode. When RESET is pushed, that bit returns to its normally high state. CBL/BYTE/BIT is selected according to the following:

	RF	
ANT 1	ANT 2	ANT 3
12/3/1	12/3/2	12/3/3

	IF	
ANT 1	ANT 2	ANT 3
12/3/1	12/3/2	12/3/3

The parameter the operator enters is the Y-factor.

C = Total coupling loss in dB, entered at calibration time.

ENR = Excess Noise Ratio in dB, entered at calibration time; different for each noise diode.

Y = Entered by operator at measurement time

X = 67 MHz if IF passband is select or 247 MHz if RF is selected.

ABC = RECEIVED RF, ANT. 1 (2 or 3) or SSA IF, ANT. 1 (2 or 3) depending on RF/IF and antenna selection. These are the push button labels on the Test Unit front panel.

X and ABC are written by CPU on Task 024

Instructions to CPU for OPERATING TEMPERATURE TEST (continue)

If operator selects:	Display:
RF & Ant 1	Received RF, Ant 1
RF & Ant 2	Received RF, Ant 2
RF & Ant 3	Received RF, Ant 3
IF & Ant 1	SSA IF, Ant 1
IF & Ant 2	SSA IF, Ant 2
IF & Ant 3	SSA IF, Ant 3

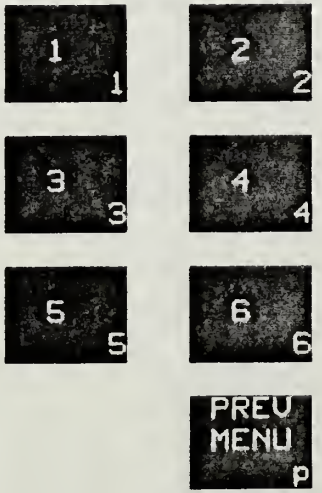
task 045 - AVAILABLE SATELLITES POWER BALANCE

Select a SATELLITE for POWER BALANCING.

1. _____ _____ 2. _____ _____

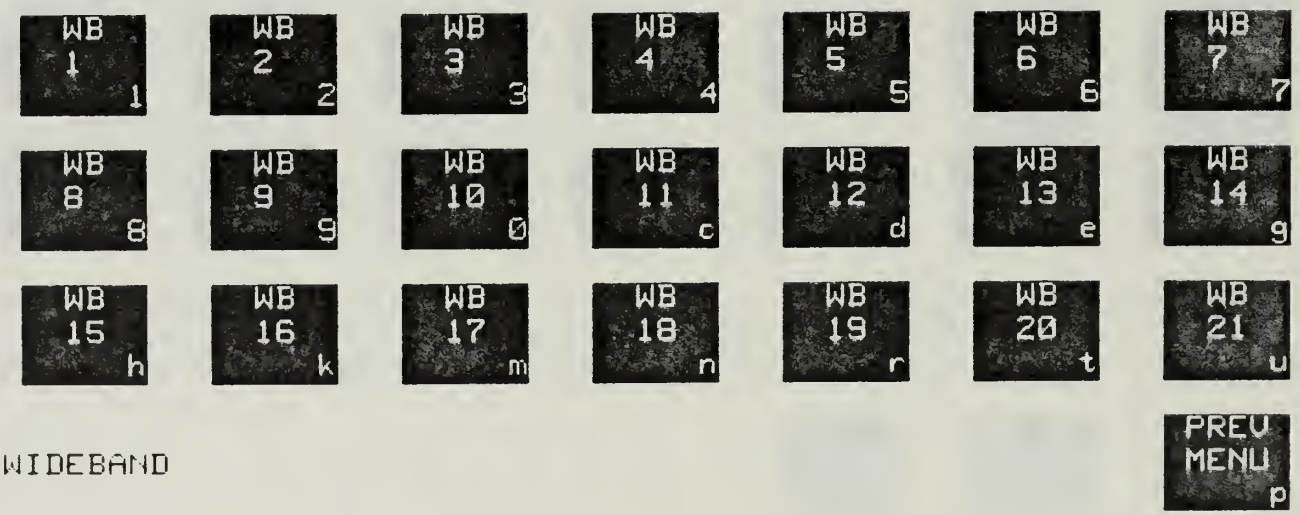
3. _____ _____ 4. _____ _____

5. _____ _____ 6. _____ _____



task047 - GAPFILLER CHANNEL SELECT POWER BALANCE

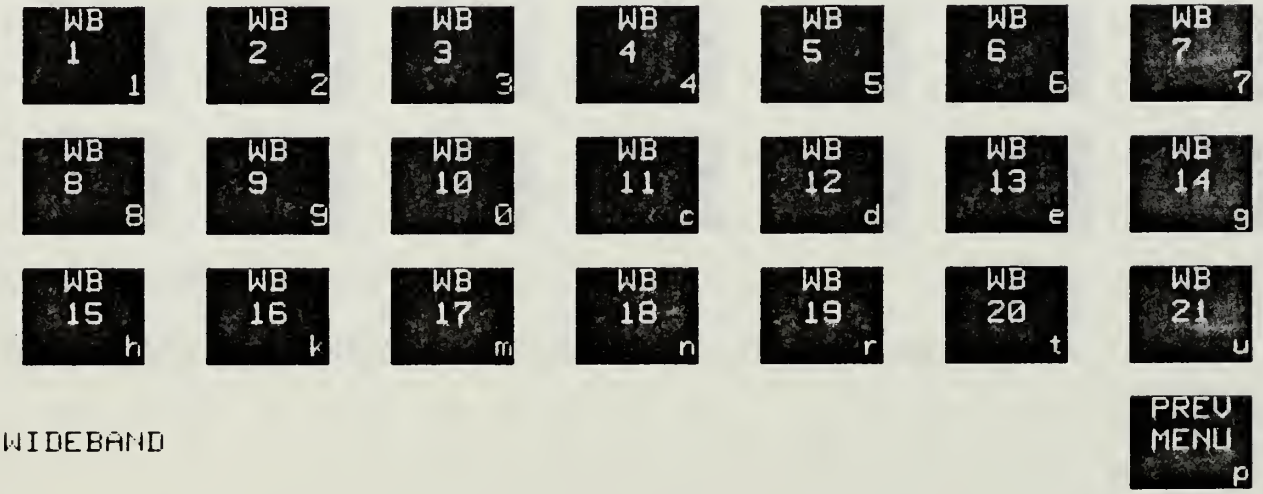
Enter the CHANNEL of the REMOTE Signal.



WB = WIDEBAND

task052 - GAPFILLER CHANNEL SELECT POWER BALANCE

Enter the CHANNEL you will use to transmit the REFERENCE signal.



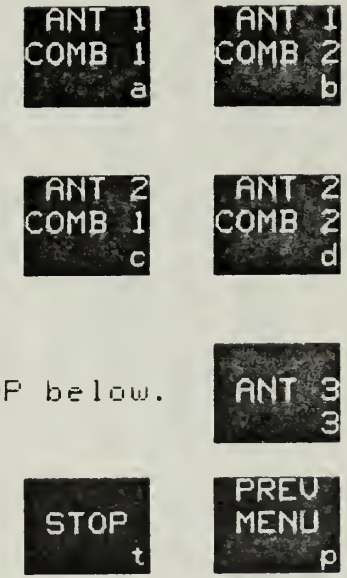
WB = WIDEBAND

task053 - POWER BALANCE INSTRUCTIONS

To do a POWER BALANCE:
1. Select ANTENNA/COMBINER for uplink.
2. Push START below.

3. Push XMTR ENABLE on TEST UNIT
   within 15 seconds.
4. Several seconds later a series of 10 EIRP
   measurements followed by their average

   will be printed.
5. Test may be halted at any time by pressing STOP below.
6. To REPEAT test, return to step 2.



Instructions to CPU for Power Balance

1. Upon selection of PBAL, CBL 12 BYTE 2, BIT 2 goes HIGH to enable XMTR.

2. Selection of a satellite fixes antenna selection. SSA will use assigned antenna for uplink and downlink. To get WSC-3 RF power to desired antenna:

CBL 11	BYTE 2	BIT	2	1
	Dummy Load -		0	0
positive true	Ant 1		0	1
	Ant 2		1	0
	Ant 3		1	1

3. Channel selection fixes frequency according to frequency plan. CBL 11 Byte 1 bits 0-7 and Byte 0, Bit 1-7 set up negative true BCD frequency selection.

4. Set up CW uplink - CBL 11 Byte 2 Bit 6 LOW = CW.
Set LO5 to 70 MHz.

5. Start power at +8dBW out of WSC-3. To adjust power, CBL11 BYTE 3

BIT	3	4	5	6	7
dB	1	2	4	8	16

WSC-3 transmits from 1dBW to 20dBW. Select desired combination of above listed db's so the sum equals desired output.

Note that Power Out of WSC-3 ≠ EIRP.

The EIRP will equal the power level we call for on the

computer plus K. K is a correction factor entered at calibration time that allows for:

a. Difference between power command from CPU and actual power out of WSC-3.

b. Cable loss from WSC-3 to antenna.

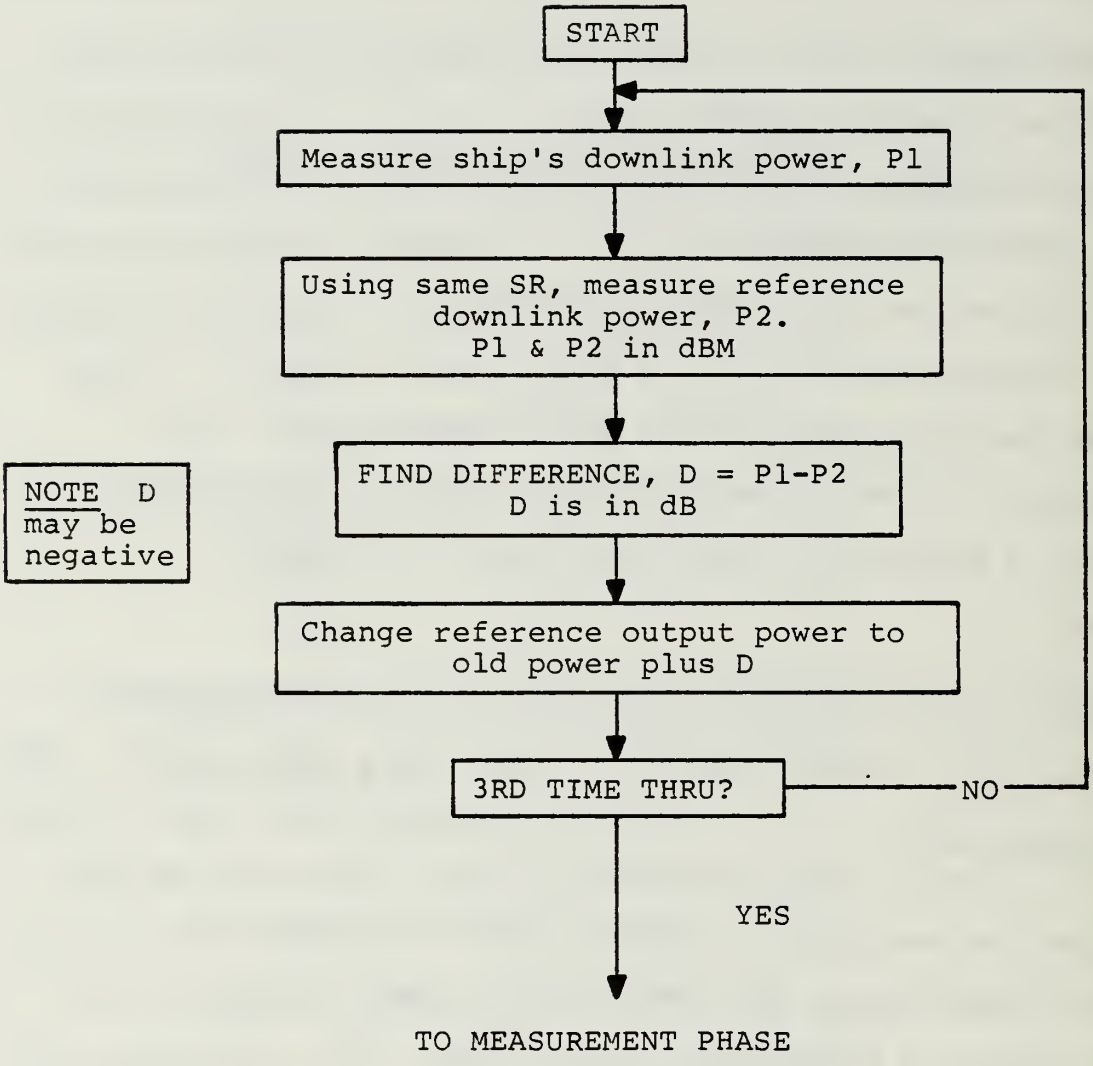
c. Antenna gain.

6. When operator pushes START, CBL12 Byte 2, bit 3 goes HIGH to key the XMTR. Just leave it turned on as long as the test is being run. Turn it off (LOW) if STOP is selected.

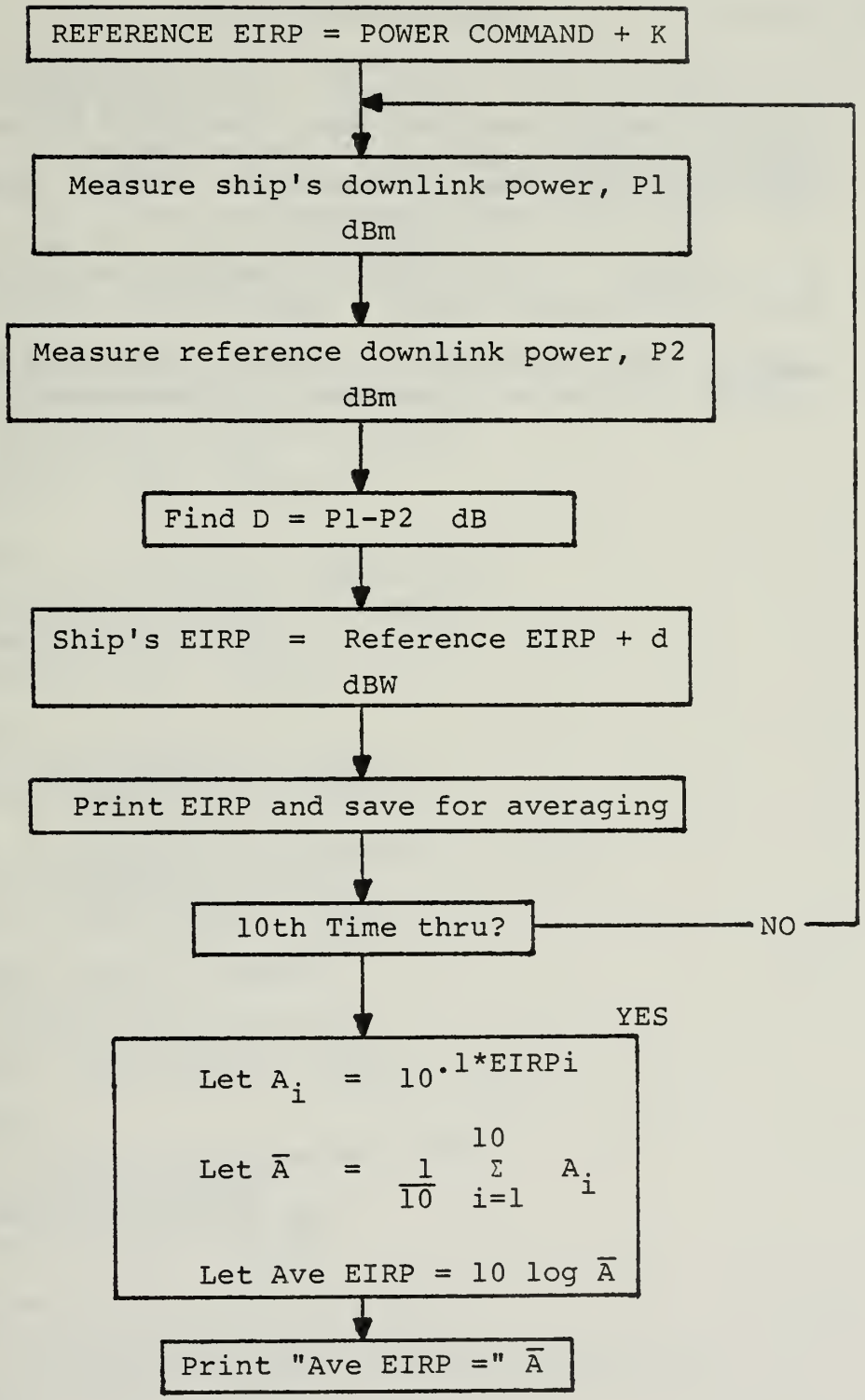
WHENEVER THE OPERATOR LEAVES THE "HOW TO DO POWER BALANCE" MENU, MAKE CBL12 BYTE 2 BITS 2 & 3 LOW. This turns off the transmitter.

7. From the computer's standpoint, PBAL is done in 2 phases. The first is the HOME-IN phase where the two power levels are made close to each other. The second is the measurement phase where CPU calculates ship's EIRP and prints it out to operator. The required operations are shown on the flow-chart that follows.

NOTE. Once transmitting is started, it will take a quarter of a second for the signal to bounce back - thus, downlink measurements should not commence for .25 second.



Power Balance "HOME-IN" PHASE



Done. Turn off
CBL 12 Byte 2 Bit 3

LIST OF REFERENCES

1. J. E. Ohlson and C. Musgrave, "Design of the Digital Control and Test Unit Subsystems for a Satellite Signal Analyzer," Project Report NPS62-79-014PR, Naval Postgraduate School, December 1979 (Unclassified), 142 pages.

2. J. E. Ohlson, "Satcom Signal Analyzer Design Review," Naval Postgraduate School, April 1979.

3. NAVELEX 0967 LP-545-4050, AN/WSC-3 Satellite Communications Transceiver Operation and Maintenance Manual.

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